EKERUCHE CHINWE BRIDGET

15/ENG02/020

COMPUTER ENGINEERING

COE506

$A(x_1\ x_2\ x_3\ x_4) = \Sigma m(3, 4, 8, 9, 11, 15)$

$B(x_1\ x_2\ x_3\ x_4) = \Sigma m(3, 4, 5, 7, 10, 14, 15)$

$C(x_1\ x_2\ x_3\ x_4) = \Sigma m(1, 5, 7, 11, 15)$

Truth table;

x_1	x_2	x_3	x_4	A	B	C
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	0
0	0	1	1	1	1	1
0	1	0	0	0	1	0
0	1	0	1	0	1	1
0	1	1	0	0	0	0
0	1	1	1	1	1	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	1	0	1
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	0	1	0
1	1	1	1	1	1	1

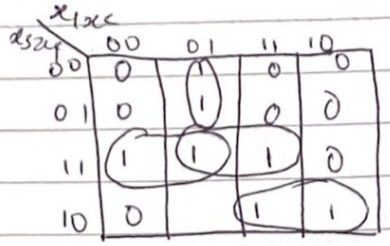
Boolean representation of the outputs A, B, C

output A;

x_3x_4 \ x_1x_2	00	01	11	10
00	0	0	0	1
01	0	0	0	1
11	1	1	1	1
10	0	0	0	0

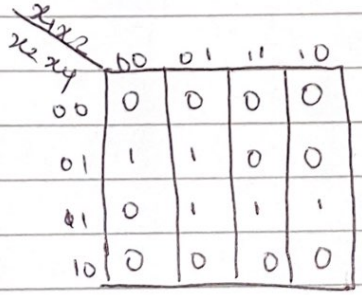
$A = x_1 \bar{x}_2 \bar{x}_3 + x_3 x_4$

output B;



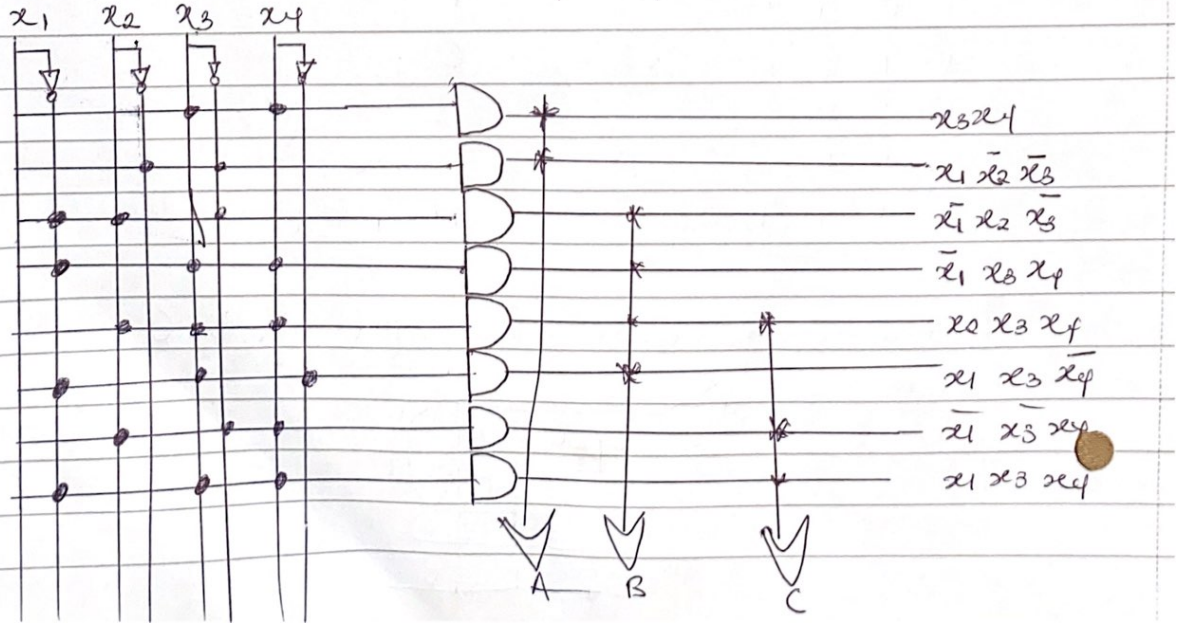
$B = \bar{x}_1 x_2 \bar{x}_3 + \bar{x}_1 x_3 x_4 + x_2 x_3 x_4 + x_1 x_3 \bar{x}_4$

Output C



$C = \bar{x}_1 \bar{x}_3 x_4 + x_2 x_3 x_4 + x_1 x_3 x_4$

⇒ logic circuit design; implementing using PLA



Number 2.

i from the logic circuit Blackbox view, we have 4 inputs to the circuit
$2^4 = 16$ states

Truth table.

S_{W1}	S_{W2}	S_{W3}	S_{W4}	x (output)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	x (dont case)
1	0	1	0	1
1	0	1	1	x (dont case)
1	1	0	0	1
1	1	0	1	x (dont case)
1	1	1	0	1
1	1	1	1	x (dont case)

ii Behavioral VHDL model for the minimized boolean expression.
In this case we would represent the following.

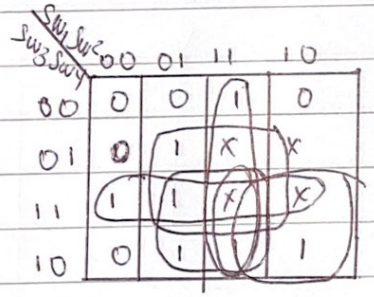
$S_{W1} = a$
$S_{W2} = b$
$S_{W3} = c$
$S_{W4} = d$
} input.

$x = x$ → output.

Code;

```
libran ieee;
use ieee.std_logic_1164.ALL;
entity switches is
port(swa, swb, swc, swd; in std_logic; x; out std_logic);
end switches

Architecture data flow of switches is begin.
  x <= (swc and swd) or
       (swa and swb) or
       (swb and swd) or
       (swa and swc);
end data flow;
```



$X = Sw3Sw4 + Sw1Sw2 + Sw2Sw4 + Sw1Sw3$