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Mat No : 15/Eng02/035

1) $A(x_1 x_2 x_3 x_4) = \Sigma m(3, 7, 8, 9, 11, 18)$
$B(x_1 x_2 x_3 x_4) = \Sigma m(3, 4, 5, 7, 10, 14, 15)$
$C(x_1 x_2 x_3 x_4) = \Sigma m(1, 5, 7, 11, 15)$

Truth table

x_1	x_2	x_3	x_4	A	B	C
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	0
0	0	1	1	1	1	0
0	1	0	0	0	1	0
0	1	0	1	0	1	1
0	1	1	0	0	0	0
0	1	1	1	1	1	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	1	0	1
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	0	1	0
1	1	1	1	1	1	1

Boolean Representation Of the Outputs A, B and C

Output A;

x_3x_4 \ x_1x_2	00	01	11	10
00	0	0	0	1
01	0	0	0	1
11	1	1	1	1
10	0	0	0	0

$$A = x_1 \bar{x}_2 \bar{x}_3 + x_3 x_4$$

Output B

x_3x_4 \ x_1x_2	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	1	1	1	0
10	0	0	1	1

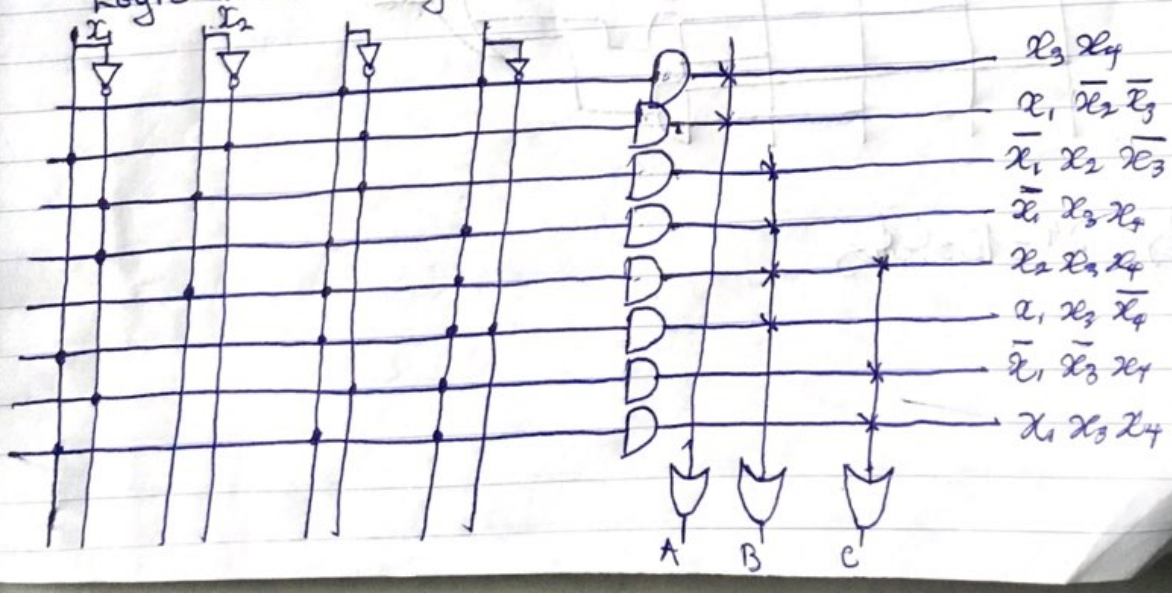
$$B = \bar{x}_1 x_2 \bar{x}_3 + \bar{x}_1 x_3 x_4 + x_2 x_3 x_4 + x_1 x_3 \bar{x}_4$$

Output C

x_3x_4 \ x_1x_2	00	01	11	10
00	0	0	0	0
01	1	1	0	0
11	0	1	1	1
10	0	0	0	0

$$C = \bar{x}_1 \bar{x}_3 x_4 + x_2 x_3 x_4 + x_1 x_3 x_4$$

Logic circuit design

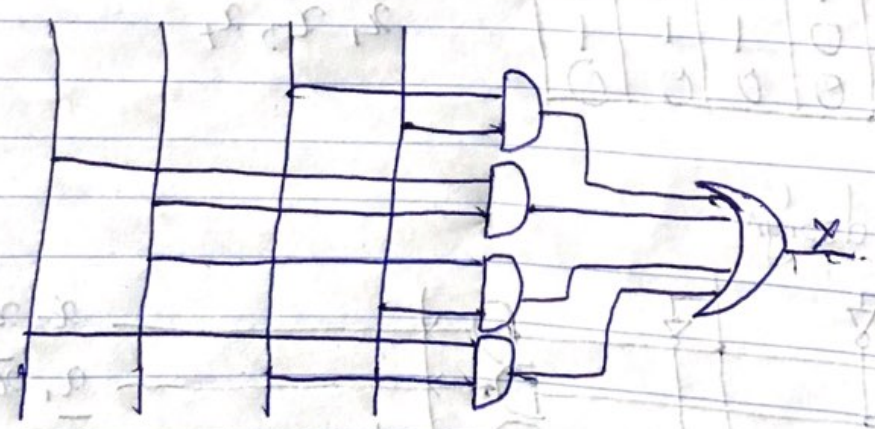


Code

```
library ieee;
use ieee.std_logic_1164.all;
entity switches is
port (swa, swb, swc, swd : in std_logic;
  x : out std_logic);
end switches
Architecture data flow of switches is begin
  x <= (swc and swd) or
       (swa and swb) or
       (swb and swd) or
       (swa and swc);
end data flow
```

$sw_3 sw_4$ \ $sw_1 sw_2$	00	01	11	10
00	0	0	1	0
01	1	1	X	X
11	1	1	X	X
10	0	1	1	1

$x = sw_3 sw_4 + sw_1 sw_2 + sw_2 sw_4 + sw_1 sw_3$



2d) $2^4 = 16$ states

Truth table

Sw1	Sw2	Sw3	sw4	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	X
1	0	1	0	1
1	0	1	1	X
1	1	0	0	1
1	1	0	1	X
1	1	1	0	1
1	1	1	1	X