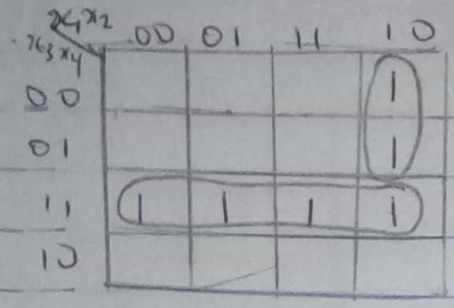
QUESTION ONE

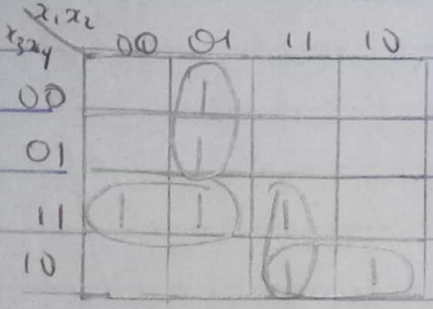
$A(x_1\ x_2\ x_3\ x_4) = \Sigma m(3, 7, 8, 9, 11, 15)$

$B(x_1\ x_2\ x_3\ x_4) = \Sigma m(3, 4, 5, 7, 10, 14, 15$

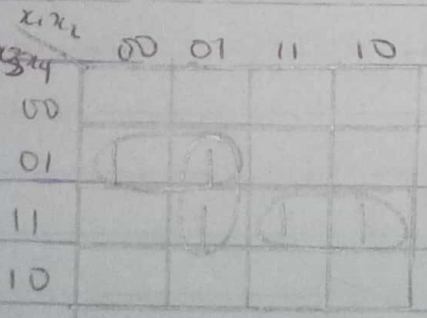
$C(x_1\ x_2\ x_3\ x_4) = \Sigma m(1, 5, 7, 11, 15)$



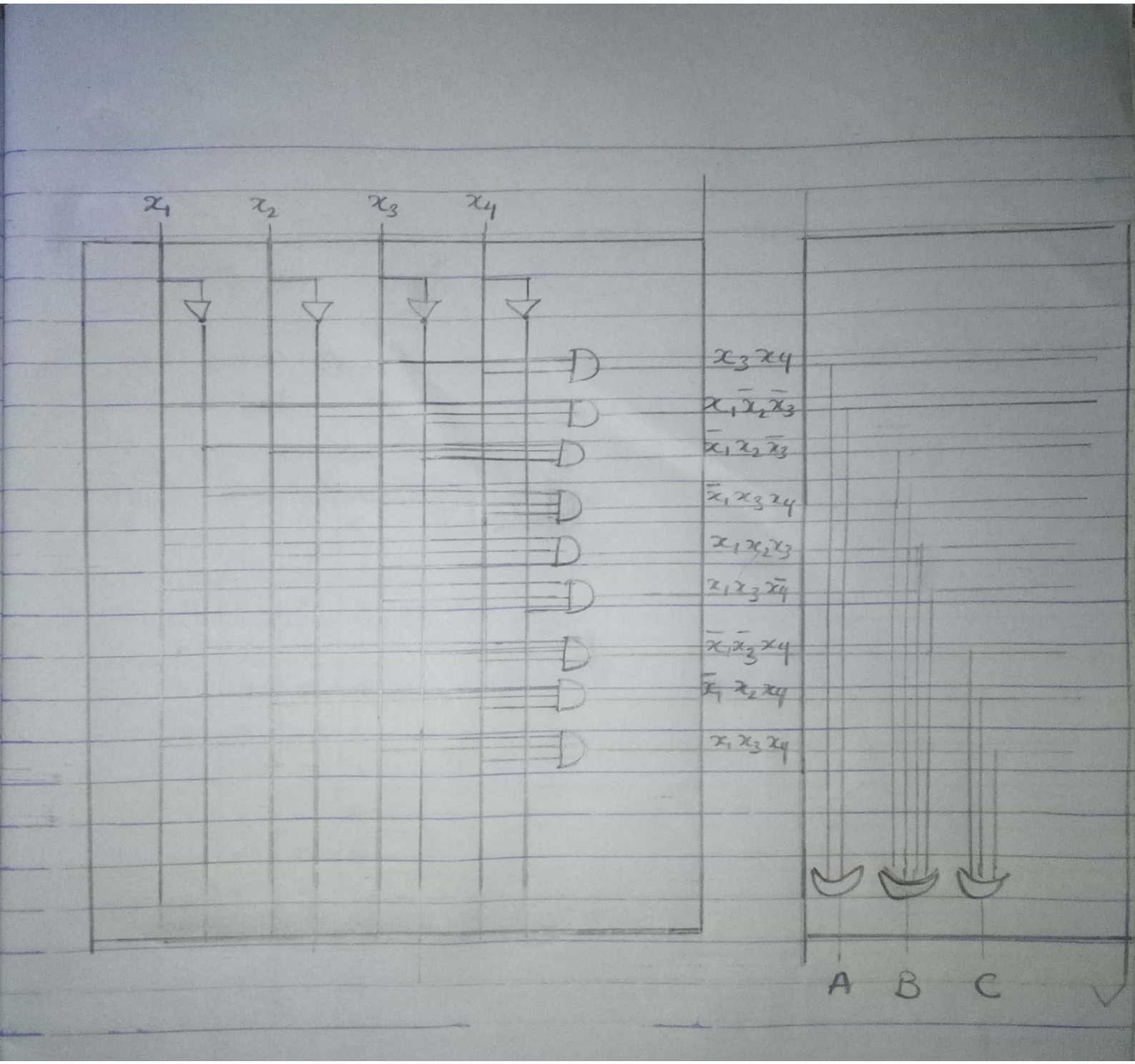
$A = x_3 x_4 + x_1 \bar{x}_2 \bar{x}_3$



$B = \bar{x}_1 x_2 \bar{x}_3 + \bar{x}_1 x_3 x_4 + x_1 x_2 x_3 + x_1 x_3 \bar{x}_4$



$C = \bar{x}_1 \bar{x}_3 x_4 + \bar{x}_1 x_2 x_4 + x_1 x_3 x_4$.

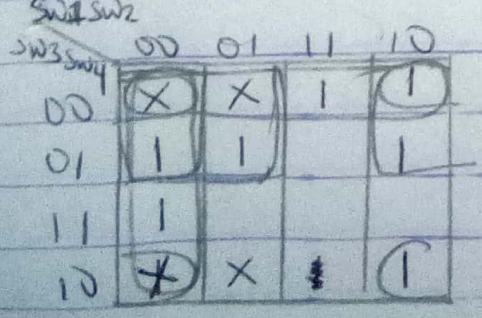


QUESTION TWO

* Output X is HIGH whenever two or more switches are closed (0)

* ~~SW1~~ When SW1 & SW4 are closed, we don't care about the output.

SW1	SW2	SW3	SW4	OUTPUT (X)
0	0	0	0	X
0	0	0	1	1
0	0	1	0	X
0	0	1	1	1
0	1	0	0	X
0	1	0	1	1
0	1	1	0	X
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0



$$X = \overline{SW_2}\,\overline{SW_4} + \overline{SW1}\,\overline{SW2} + \overline{SW1}\,\overline{SW3} + \overline{SW3}\,\overline{SW4} + \overline{SW2}\,\overline{SW3}$$

Behavioural VHDL model

```
Library ieee
Use ieee.std_logic_1164.all

Entity control is
port (SW1, SW2, SW3, SW4 : in std_logic;
      X : out std_logic);
end control;

Architecture logic of control is
begin

X <= (SW2 NAND SW4) OR (SW1 NAND SW2) OR
     (SW1 NAND SW3) OR (SW3 NAND SW4) OR
     (SW2 NAND SW3);

end logic;
```