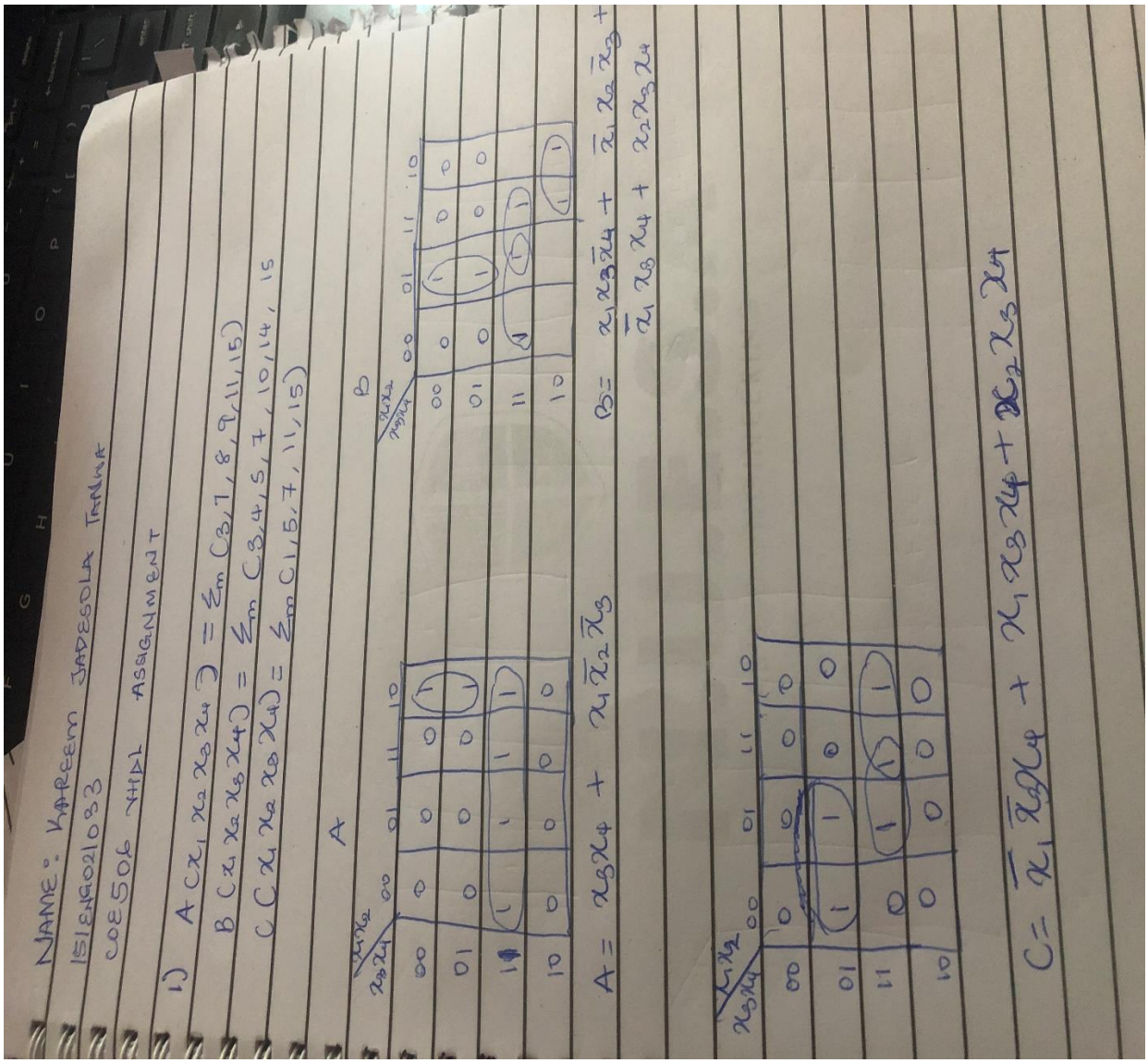
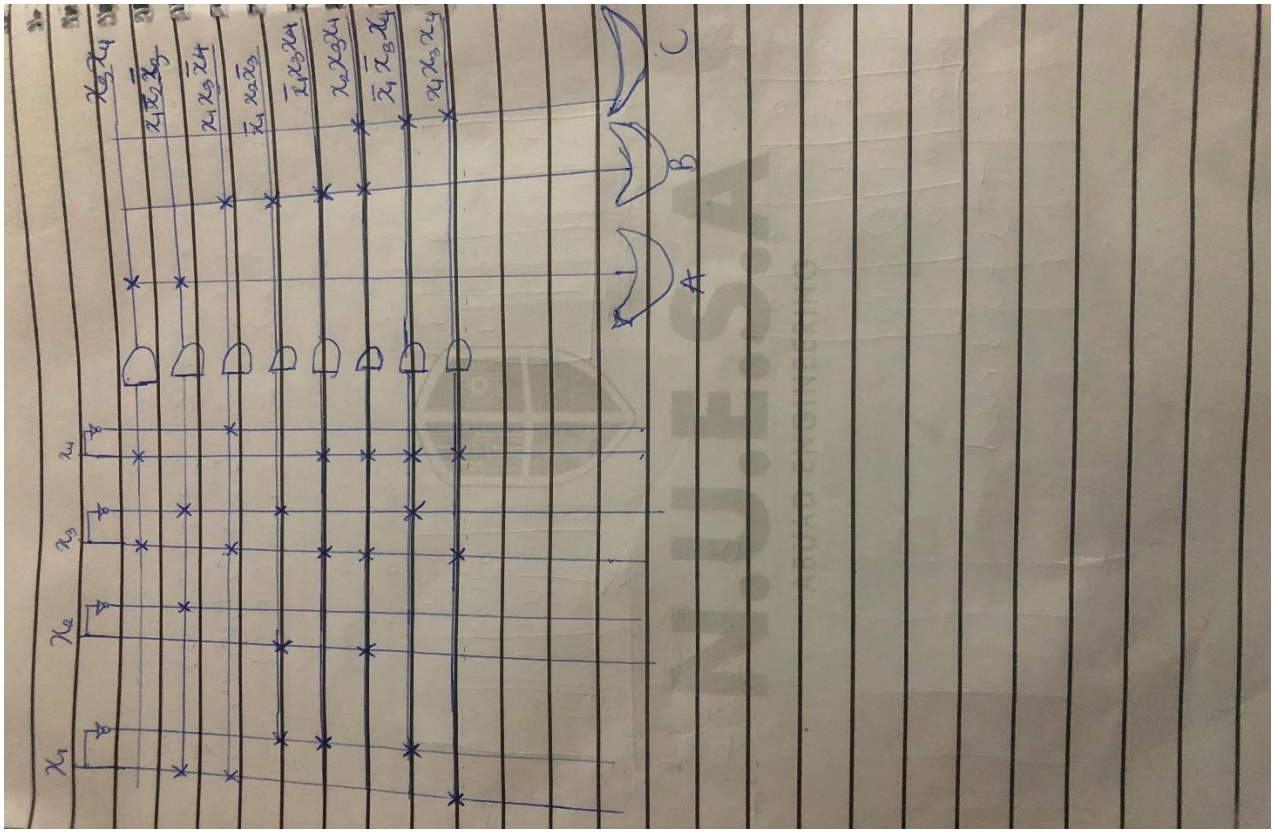
NAME: KAREEM JADESOLA ‘TANWA

15/ENG02/033

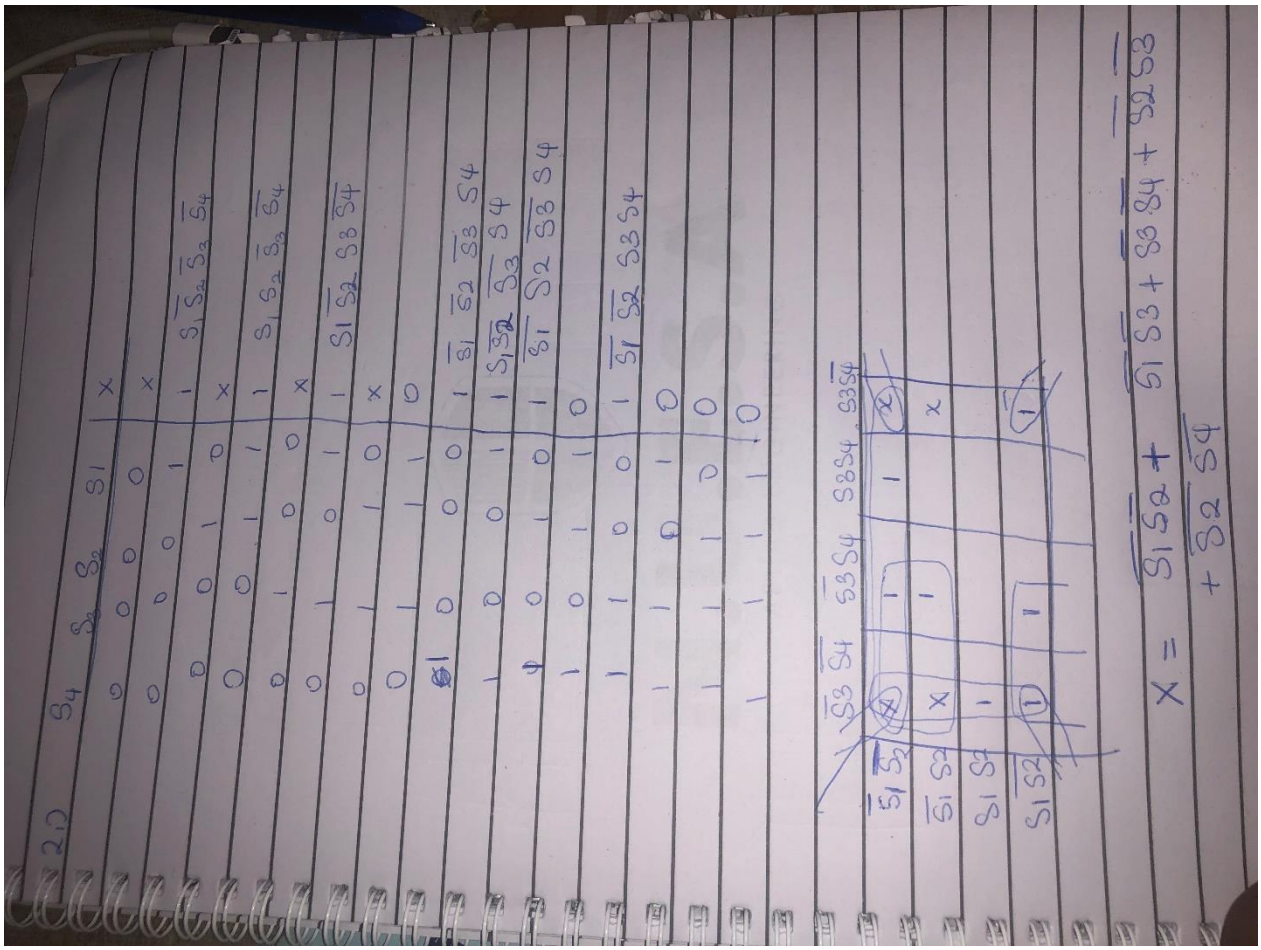
COE506 VHDL ASSIGNMENT.

1.





2i.



2ii.library ieee;

use ieee.std_logic_1164.all;

entity control_circuitry_model is

port (S1, S2, S3, S4: in std_logic; X: out std_logic);

end control_circuitry_model;

architecture behavioral of control_circuitry_model is

begin

X <= (S2 NAND S4) or (S1 NAND S2) or (S1 NAND S3) or (S3 NAND S4) or (S2 NAND S3);

end behavioral;