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15/ENG02/033

COE506 VHDL ASSIGNMENT.

1.

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 15ENG021033
 COE506 VHDL ASSIGNMENT

1) $A(x_1, x_2, x_3, x_4) = \sum_m (3, 7, 8, 9, 11, 15)$
 $B(x_1, x_2, x_3, x_4) = \sum_m (3, 4, 5, 7, 10, 14, 15)$
 $C(x_1, x_2, x_3, x_4) = \sum_m (1, 5, 7, 11, 15)$

A

x_3x_4 x_2x_1	00	01	11	10
00	0	0	0	1
01	0	0	0	0
11	1	1	1	1
10	0	0	0	0

$A = x_3x_4 + x_1\bar{x}_2\bar{x}_3$

B

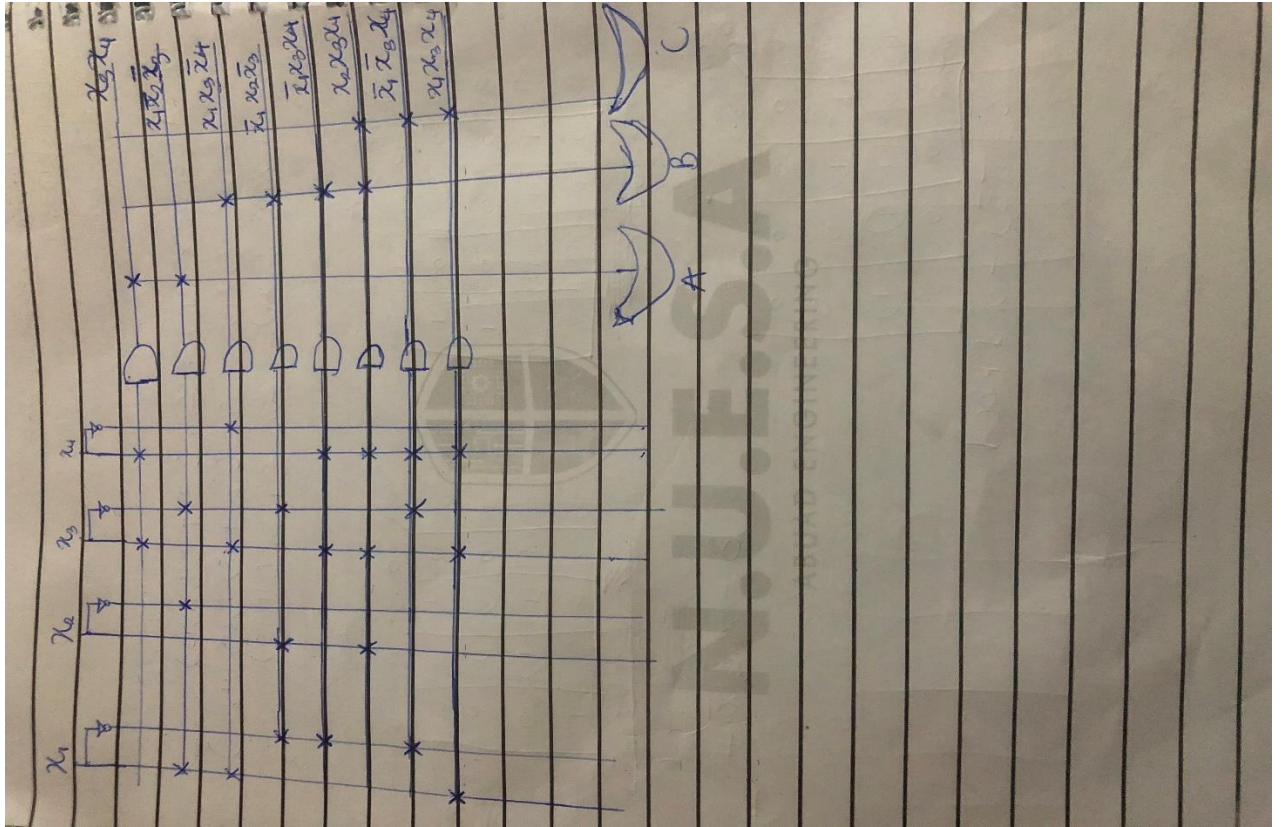
x_3x_4 x_2x_1	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	1	1	1	1
10	0	0	0	1

$B = x_1x_3\bar{x}_4 + \bar{x}_1x_3x_4 + x_2x_3x_4$

C

x_3x_4 x_2x_1	00	01	11	10
00	0	0	0	0
01	1	1	0	0
11	0	1	1	1
10	0	0	0	0

$C = \bar{x}_1\bar{x}_2x_4 + x_1x_3x_4 + x_2x_3x_4$



2i.

S_1	S_2	S_3	S_4	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	0	1	0
0	1	0	0	0
0	0	1	0	0
0	1	0	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	0	0
1	1	1	1	0

S_1	S_2	S_3	S_4	X
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

$$X = \overline{S_1 S_2} + \overline{S_1 S_3} + \overline{S_1 S_4} + \overline{S_2 S_3} + \overline{S_2 S_4}$$

```
2ii.library ieee;
use ieee.std_logic_1164.all;
entity control_circuitry_model is
    port (S1, S2, S3, S4: in std_logic; X: out std_logic);
end control_circuitry_model;
architecture behavioral of control_circuitry_model is
begin
X <= (S2 NAND S4) or (S1 NAND S2) or (S1 NAND S3) or (S3 NAND S4) or (S2
NAND S3);
end behavioral;
```