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15/ENG02/043

COE 506 Assignment.

- ①  $A(x_1, x_2, x_3, x_4) = \sum m(3, 7, 8, 9, 11, 15)$   
 $B(x_1, x_2, x_3, x_4) = \sum m(3, 4, 5, 7, 10, 14, 15)$   
 $C(x_1, x_2, x_3, x_4) = \sum m(1, 5, 7, 11, 15)$

Truth Table:

$x_1$	$x_2$	$x_3$	$x_4$	A	B	C
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	0
0	0	1	1	1	1	0
0	1	0	0	0	1	0
0	1	0	1	0	1	1
0	1	1	0	0	0	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	1	0	1
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	0	1	0
1	1	1	1	1	1	1
1	1	1	1	1	1	1

Boolean representation of the outputs A, B and C.

Output A :

$x_3 \backslash x_2$	$x_1$	00	01	11	10
00	0	0	0	0	1
01	0	0	0	0	1
11	1	1	1	1	1
10	0	0	0	0	0

$$A = X_1 \bar{X}_2 \bar{X}_3 + X_3 X_4$$

Output B :

$x_3 \backslash x_2$	$x_1$	00	01	11	10
00	0	1	0	0	0
01	0	1	0	0	0
11	1	1	1	0	0
10	0	1	1	1	0

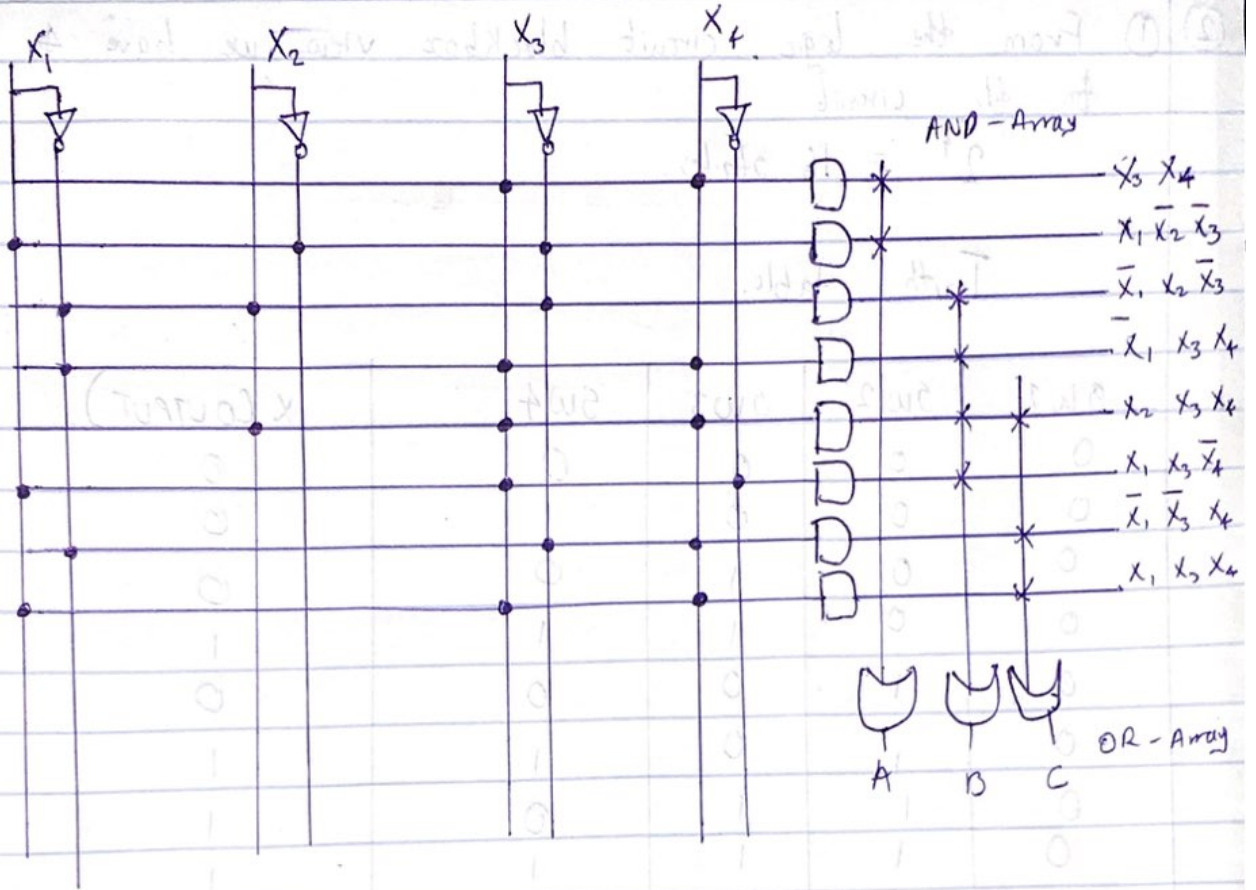
$$B = \bar{X}_1 X_2 \bar{X}_3 + \bar{X}_1 X_3 X_4 + X_2 X_3 X_4 + X_1 X_3 \bar{X}_4$$

Output C :

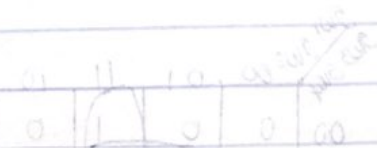
$x_3 \backslash x_2$	$x_1$	00	01	11	10
00	0	0	0	0	0
01	1	1	0	0	0
11	0	1	1	1	0
10	0	0	0	0	0

$$C = \bar{X}_1 \bar{X}_3 X_4 + X_2 X_3 X_4 + X_1 X_3 X_4$$

⇒ Logic Circuit Design : Implementing using PLA.



(500) (100) x  
 (500) (100) x  
 (500) (100) x  
 (500) (100) x



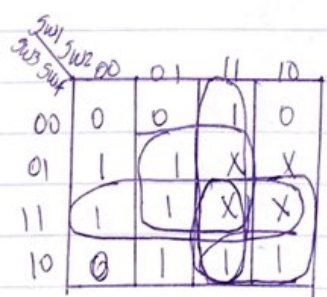
Logic Circuit Design - Implementing a Logic Function

② ① From the logic circuit blackbox view we have 4 inputs to the circuit

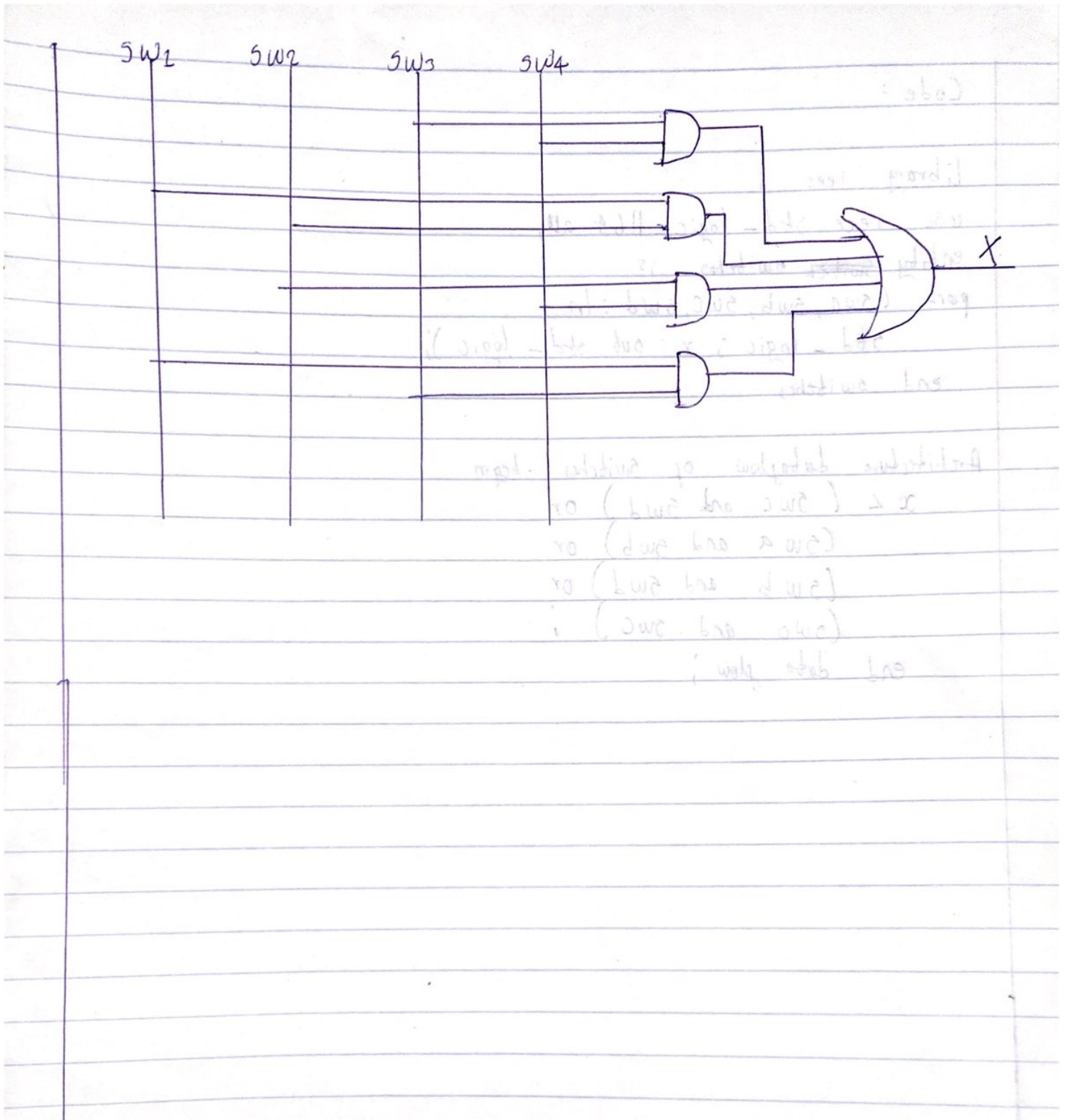
$2^4 = 16$  states.

Truth table.

SW1	SW2	SW3	SW4	X (OUTPUT)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	X (don't care)
1	0	1	0	1
1	0	1	1	X (don't care)
1	1	0	0	1
1	1	0	1	X (don't care)
1	1	1	0	1
1	1	1	1	X (don't care)



$X = SW3SW4 + SW1SW2 + SW2SW4 + SW1SW3$



Code :

```
library ieee ;  
use ieee.std_logic_1164.all;  
entity switch switches is  
port (swa, swb, swc, swd : in  
      std_logic ; x : out std_logic);  
end switches
```

Architecture Datapath of switches .begin

```
x < ( swc and swd ) or  
    ( swa and swb ) or  
    ( swb and swd ) or  
    ( swa and swc ) ;  
end data flow ;
```