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15/MHS01/012
Computer Engineering

Code:

```
library ieee;
use ieee.std_logic_1164.all;
entity switches is
port (swa, swb, swc, swd : in
std_logic; X: out std_
logic);

end switches.

Architecture dataflow of switches is
begin
X <= (swc and swd) or
     (swa and swb) or
     (swa and swc);
end dataflow;
```

| swa swb \ swc swd | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 1 | 0 |
| 01 | 0 | 1 | X | X |
| 11 | 1 | 1 | X | X |
| 10 | 0 | 1 | 1 | 1 |

$X = SW_3 SW_4 + SW_1 SW_2 + SW_2 SW_4 + SW_1 SW_3$