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15/ENG02/002
COE 506 Assignment

1) $A(X_1 X_2 X_3 X_4) = \sum m(3,7,8,9,11,15)$

$B(X_1, X_2, X_3, X_4) = \sum m(3,4,5,7,10,14,15)$

$C(X_1, X_2, X_3, X_4) = \sum m(1,5,7,11,15)$ .

TRUTH TABLE

| $X_1$ | $X_2$ | $X_3$ | $X_4$ | A | B | C |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Representation of A

output A :-

| $X_3X_4$ \ $X_1X_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 1 |
| 01 | 0 | 0 | 0 | 1 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 0 | 0 | 0 | 0 |

$$A = X_1\overline{X}_2\overline{X}_3 + X_3X_4$$

Output B :-

| $X_3X_4$ \ $X_1X_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 0 | 0 |
| 01 | 0 | 1 | 0 | 0 |
| 11 | 1 | 1 | 1 | 0 |
| 10 | 0 | 0 | 1 | 1 |

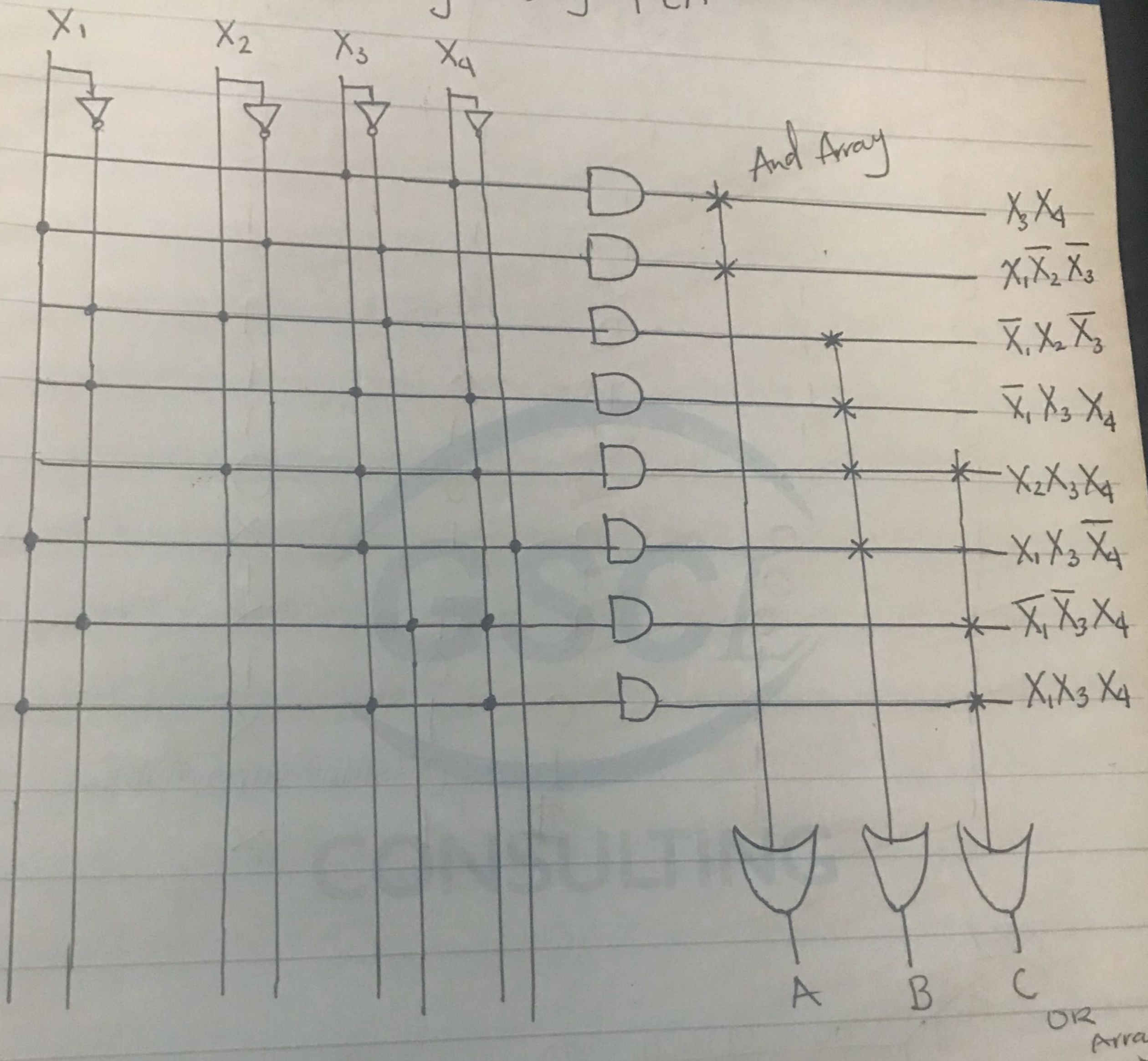
$$B = \overline{X}_1X_3X_4 + \overline{X}_1X_2\overline{X}_3 + X_2X_3X_4 + X_1X_3\overline{X}_4$$

utput C :-

| $X_3X_4$ \ $X_1X_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 0 |
| 01 | 1 | 1 | 0 | 0 |
| 11 | 0 | 1 | 1 | 1 |
| 10 | 0 | 0 | 0 | 0 |

$$C = X_1X_3X_4 + \overline{X}_1\overline{X}_3X_4 + X_2X_3X_4$$

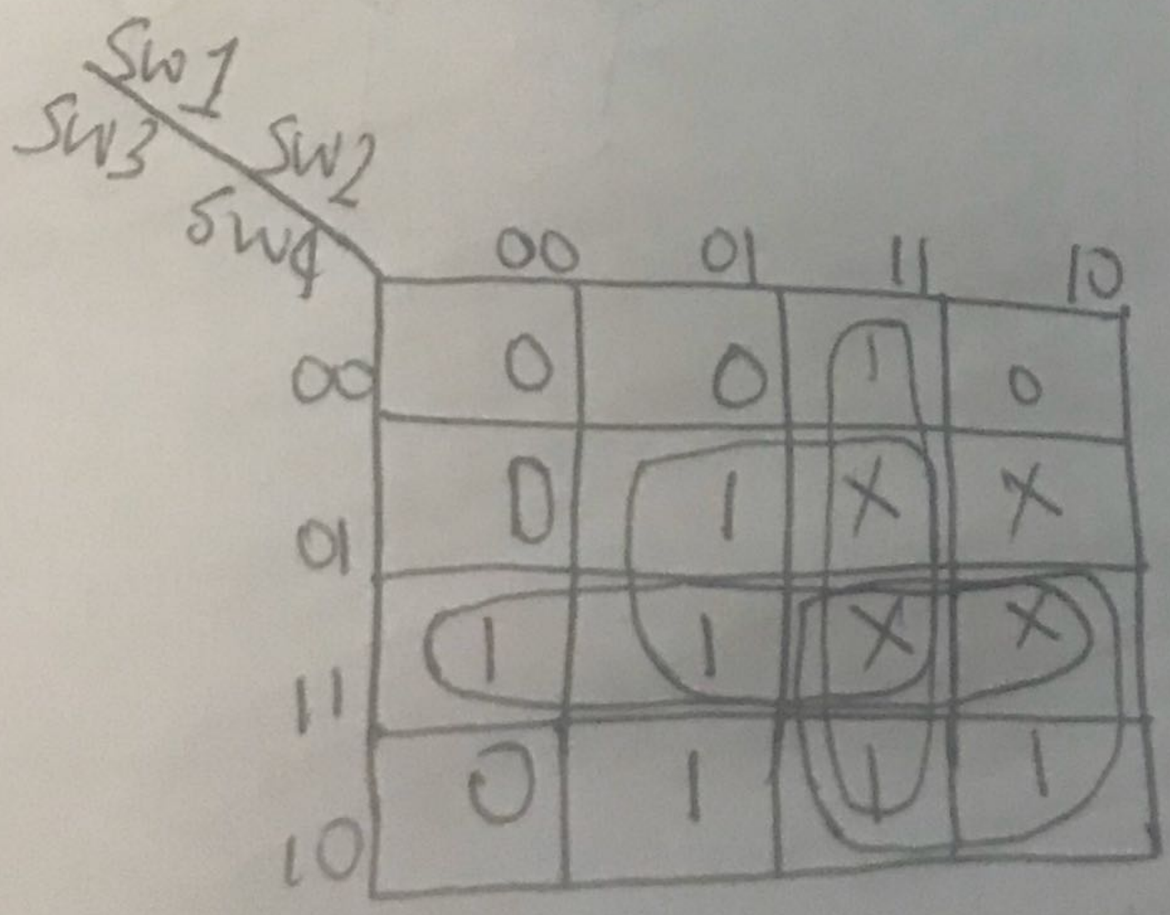
# logic circuit design using PLA



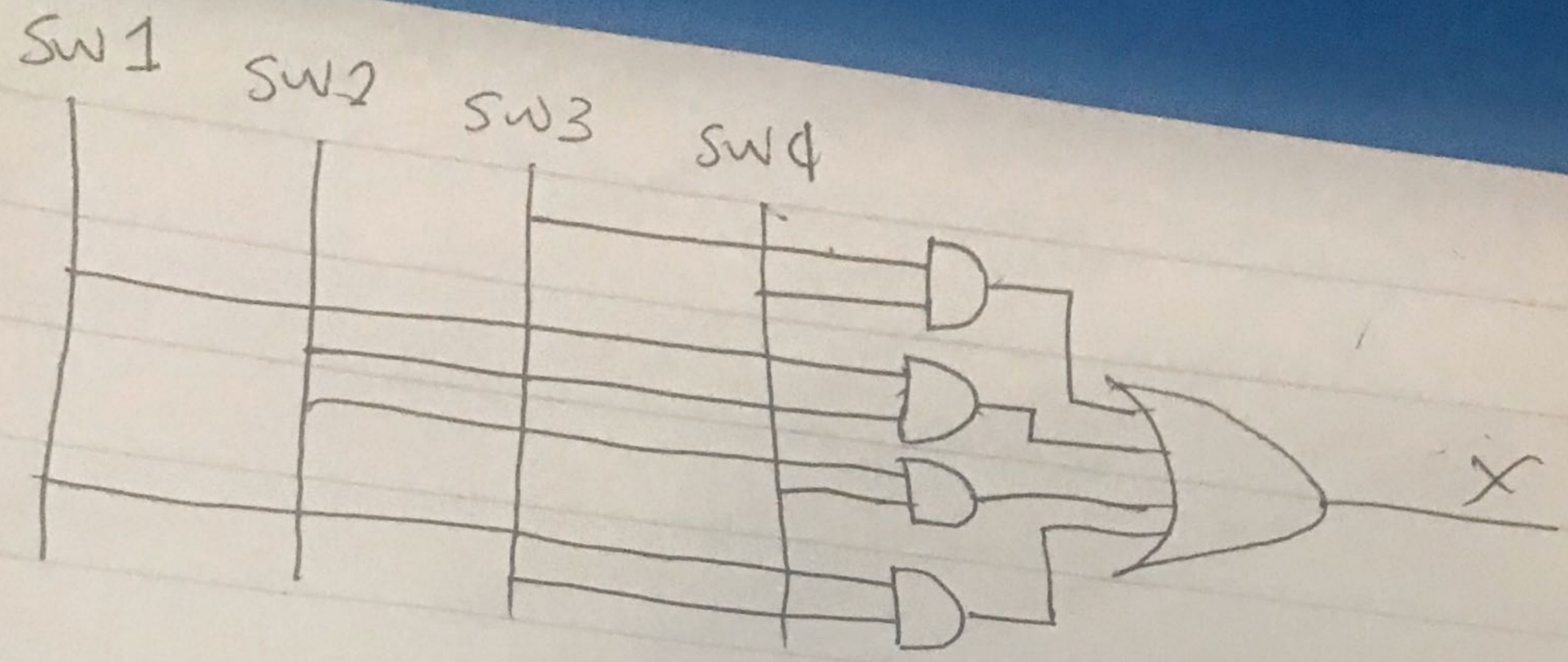
3) 4 inputs = 16 states ($2^4$)

Truth table

| SW1 | SW2 | SW3 | SW4 | X (output) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | X |
| 0 | 1 | 1 | 1 | X |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | X |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | X |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | X |




$$X = SW_3SW_4 + SW_1SW_2 + SW_1SW_3 + SW_2SW_4$$




Coding

```
library ieee;
use ieee.std_logic_1164.all;
entity switches is
port (swa, swb, swc, swd : in std_logic; x: out
      std_logic);
end switches
```

```
Architecture dataflow of switches is
x <= ((swc and swd) or (swa and swb) or
     (swb and swd) or (swa and swc);
end dataflow;
```