FAROUK UMAR FAROUK
15/ENG02/025 COE 506

1) $A(x_1x_2x_3x_4) = \Sigma m(3, 7, 8, 9, 11, 1$

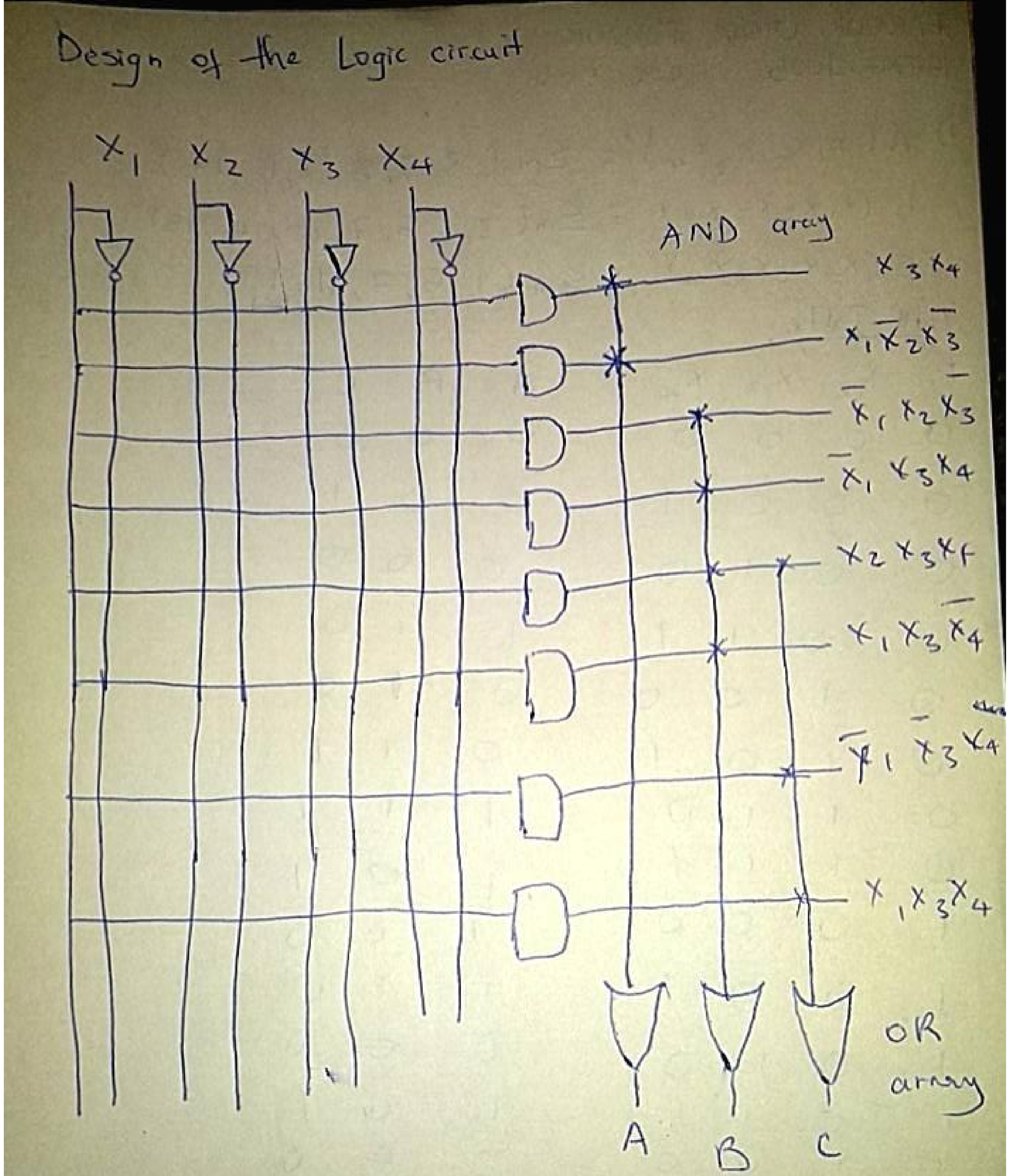
$B(x_1x_2x_3x_4) = \Sigma m(3, 4, 5, 7, 10, 14$

$C(x_1x_2x_3x_4) = \Sigma m(1, 5, 7, 11, 15)$

Truth Table:

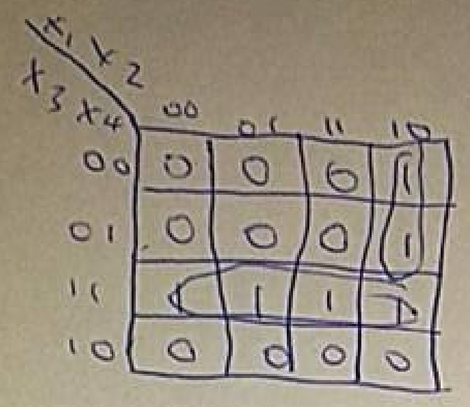
x_1	x_2	x_3	x_4	A	B	C
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	0
0	0	1	1	1	1	1
0	1	0	0	1	0	0
0	1	0	1	1	1	1
0	1	1	0	1	0	0
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	0	1	0	1	1
1	0	1	0	0	0	0
1	0	1	1	1	1	1
1	1	0	0	0	0	0
1	1	0	1	0	1	1
1	1	1	0	0	0	0
1	1	1	1	1	1	1

Design of the Logic circuit



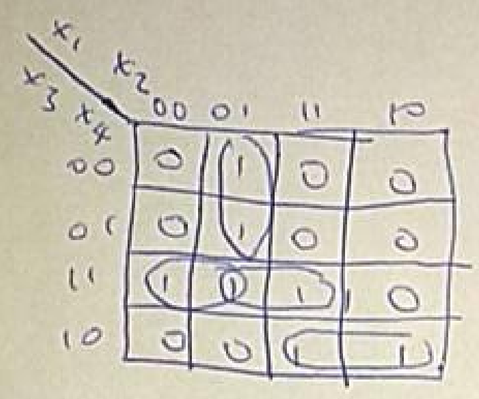
Boolean representation

output A:



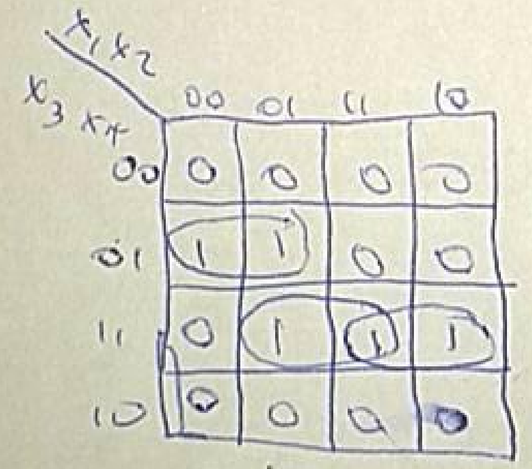
$A = x_1 \bar{x}_2 \bar{x}_3 + x_3 x_4$

output B:



$B = \bar{x}_1 x_2 \bar{x}_3 + \bar{x}_1 x_3 x_4 + x_2 x_3 x_4 + x_1 x_3 \bar{x}_4$

Output C



$C = \bar{x}_1 \bar{x}_3 x_4 + x_2 x_3 x_4 + x_1 x_3 x_4$

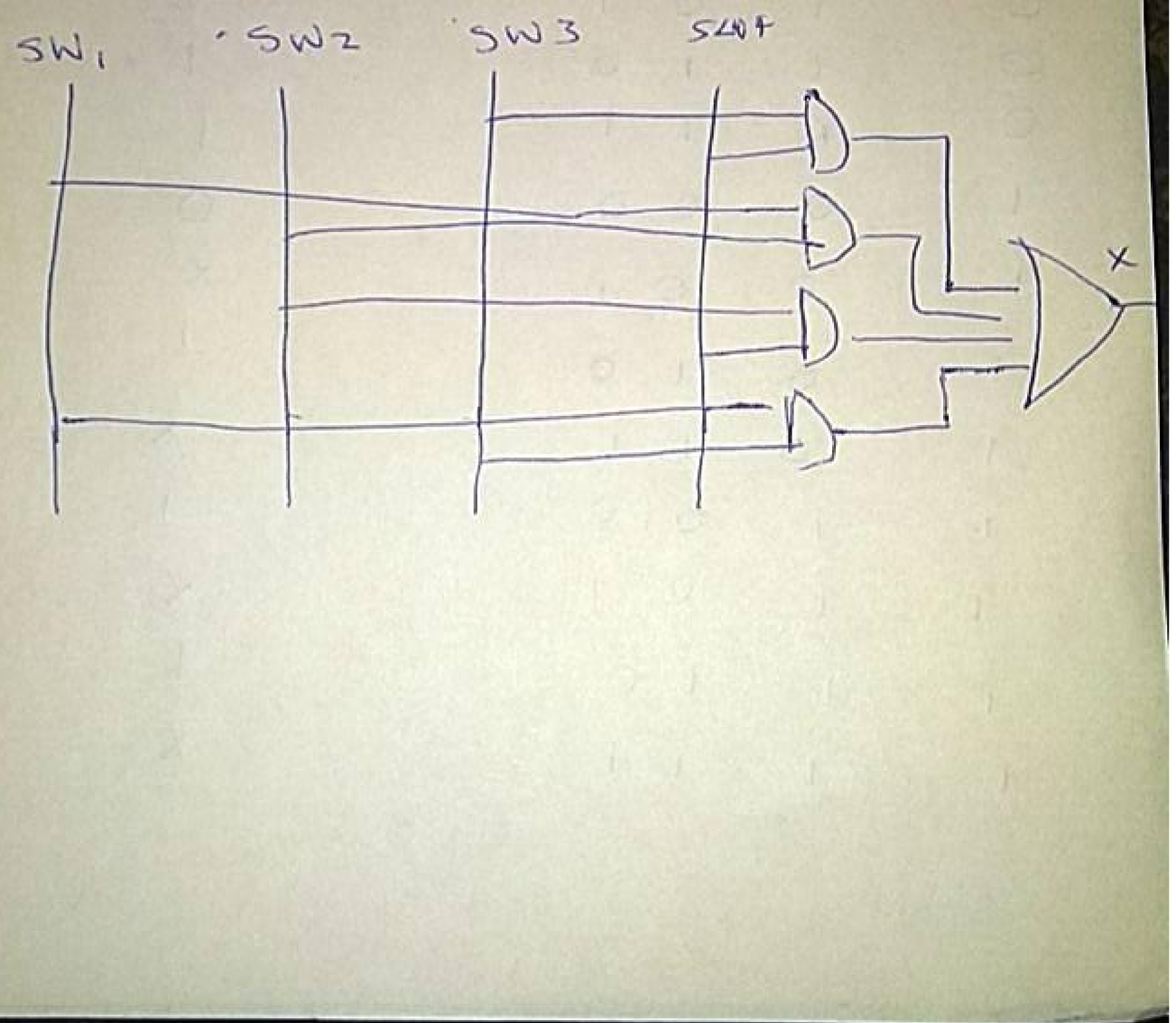
2) i

Truth Table

SW1	SW2	SW3	SW4	X (output)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	X
1	0	0	1	1
1	0	1	0	X
1	0	1	1	1
1	1	0	0	X
1	1	0	1	1
1	1	1	0	X
1	1	1	1	X

SW1 SW2 / SW3 SW4	00	01	11	10
00	0	0	1	0
01	1	1	X	X
11	1	1	X	X
10	0	1	1	1

$X = SW3\,SW4 + SW_1\,SW2 + SW2\,SW4 + SW1\,SW3$



CODE

```
library ieee;
use ieee.std_logic_1164.All;
entity switches is
port (swa, swb, swc, swd : in std_logic; x:
out std_logic);
end switches

Architecture dataflow of switches:

begin
x <= (swc and swd) or
     (swa and swb) or
     (swb and swd) or
     (swa and swc);
end data flow.
```