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Course Code: COE 506

1) Designing a system using the functions Below;

$A(x_1 x_2 x_3 x_4) = \Sigma m\,(3, 7, 8, 9, 11, 15)$

$B(x_1 x_2 x_3 x_4) = \Sigma m\,(3, 4, 5, 7, 10, 14, 15)$

$C(x_1 x_2 x_3 x_4) = \Sigma m\,(1, 5, 7, 11, 15)$

Solution

1) ~~Design~~ Creating the Truth Table

S/N	x_1	x_2	x_3	x_4	A	B	C
0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	1
2	0	0	1	0	0	0	0
3	0	0	1	1	1	1	0
4	0	1	0	0	0	1	0
5	0	1	0	1	0	1	1
6	0	1	1	0	0	0	0
7	0	1	1	1	1	1	1
8	1	0	0	0	1	0	0
9	1	0	0	1	1	0	0
10	1	0	1	0	0	1	0
11	1	0	1	1	1	0	1
12	1	1	0	0	0	0	0
13	1	1	0	1	0	0	0
14	1	1	1	0	0	1	0
15	1	1	1	1	1	1	1

2) K-Mapping and Deriving Boolean expressions

-> For A:

x_3x_4 \ x_1x_2	00	01	11	10
00	0	0	0	1
01	0	0	0	1
11	1	1	1	1
10	0	0	0	0

$A = x_1\bar{x}_2\bar{x}_3 + x_3x_4$

-> For B

x_3x_4 \ x_1x_2	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	1	1	1	0
10	0	0	1	1

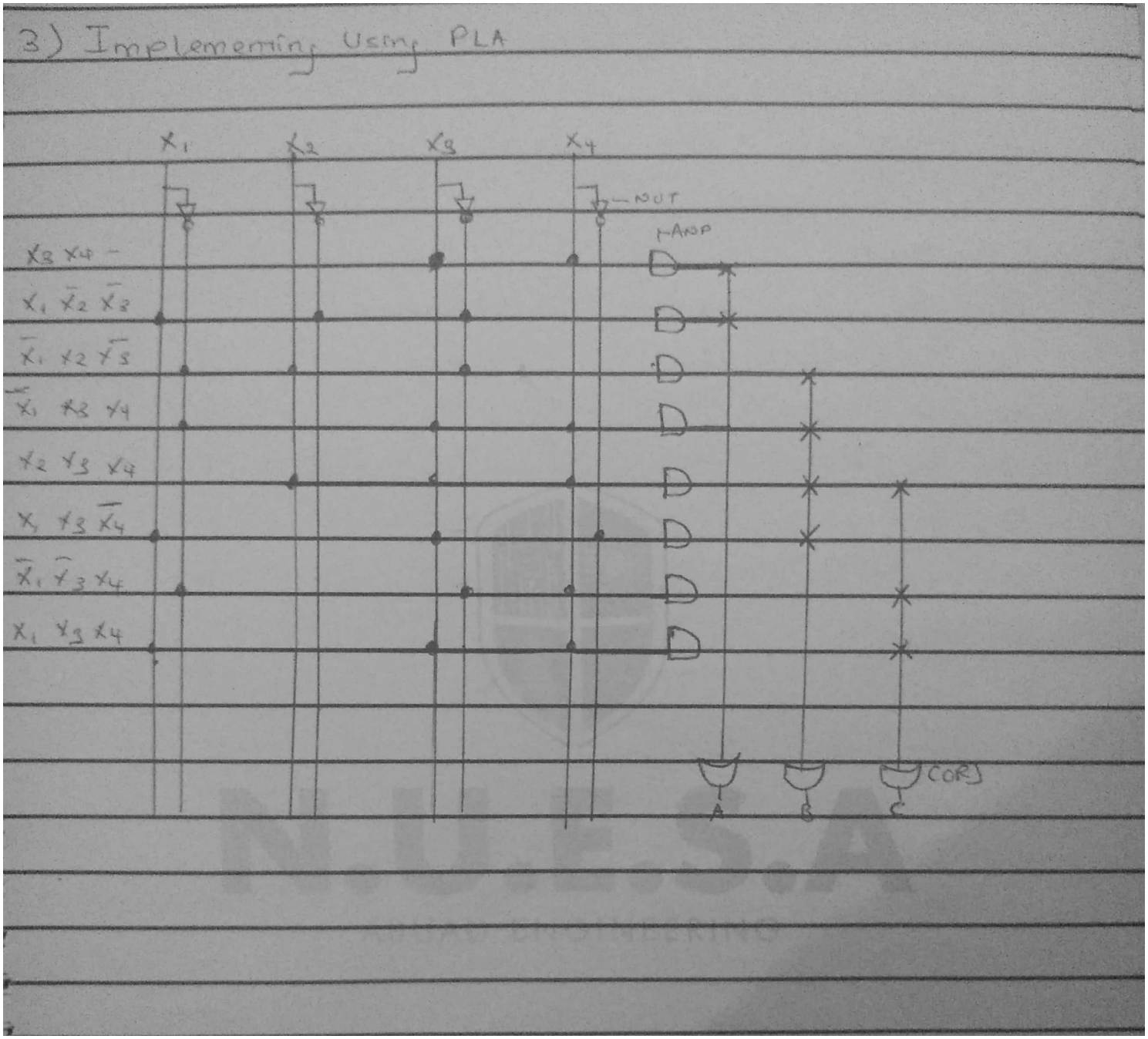
$B = \bar{x}_1x_2\bar{x}_3 + \bar{x}_1x_3x_4 + x_2x_3x_4 + x_1x_3\bar{x}_4$

-> For C

x_3x_4 \ x_1x_2	00	01	11	10
00	0	0	0	0
01	1	1	0	0
11	0	1	1	1
10	0	0	0	0

$C = \bar{x}_1\bar{x}_3x_4 + x_2x_3x_4 + x_1x_3x_4$

3) Implementing Using PLA



QUESTION 2

2) i) Design Logic Circuit to Produce HIGH output when two or more switches are closed.

ii) Write a behavioural VHDL model for minimized boolean expression

Answer

i) The Truth Table

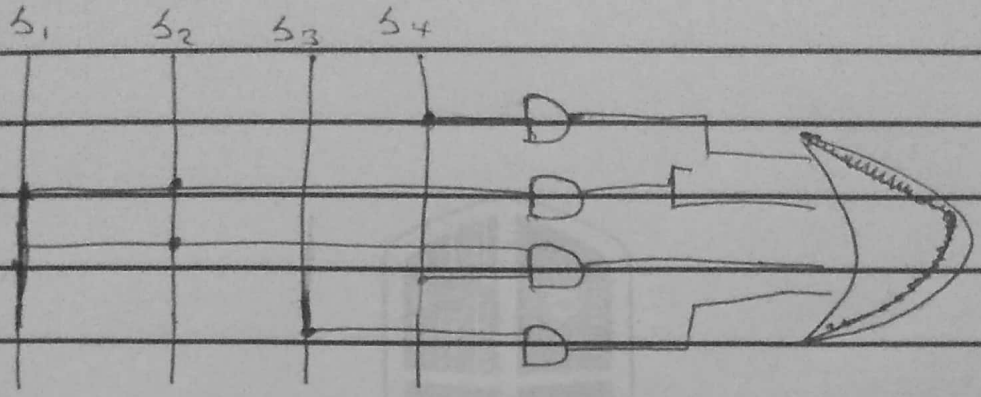
S_1	S_2	S_3	S_4	X(OUTPUT)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	x
1	0	1	0	1
1	0	1	1	x
1	1	0	0	1
1	1	0	1	x
1	1	1	0	1
1	1	1	1	x

ii) K mapping and creating Boolean expression

P.T.O

S_3S_4 \ S_1S_2	00	01	11	10
00	0	0	1	0
01	0	1	x	x
11	1	1	x	x
10	0	1	1	1

$X = S_3S_4 + S_1S_2 + S_2S_4 + S_1S_3$



1) Code for Model

```
Library ieee;
Use ieee.std_logic_1164.all;
entity Switches is
Port (S1 S2 S3 S4: In
      Std_logic; X: Out std_logic);
end switches
Architecture dataflow of Switches is
begin
  X <= (S3 and S4) or
       (S1 and S2) or
       (S2 and S4) or
       (S1 and S3);
End data flow;
```