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25/06/2020

15/ENG02/012

COE506

$$A(x_1, x_2, x_3, x_4) = \sum_m (3, 7, 8, 9, 11, 15)$$

$$B(x_1, x_2, x_3, x_4) = \sum_m (3, 4, 5, 7, 10, 14, 15)$$

$$C(x_1, x_2, x_3, x_4) = \sum_m (1, 5, 7, 11, 15)$$

Truth table.

	x_1	x_2	x_3	x_4	A	B	C
0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	1
2	0	0	1	0	0	0	0
3	0	0	1	1	1	1	0
4	0	1	0	0	0	1	0
5	0	1	0	1	0	1	1
6	0	1	1	0	0	0	0
7	0	1	1	1	1	1	1
8	1	0	0	0	1	0	0
9	1	0	0	1	1	0	0
10	1	0	1	0	0	1	0
11	1	0	1	1	1	0	1
12	1	1	0	0	0	0	0
13	1	1	0	1	0	0	0
14	1	1	1	0	0	1	0
15	1	1	1	1	1	1	1

Boolean Expressions

$$A = \bar{X}_1 \bar{X}_2 X_3 X_4 + \bar{X}_1 X_2 X_3 X_4 + X_1 \bar{X}_2 \bar{X}_3 \bar{X}_4 + X_1 \bar{X}_2 \bar{X}_3 X_4 + X_1 \bar{X}_2 X_3 X_4 + X_1 X_2 X_3 X_4$$

$$B = \bar{X}_1 \bar{X}_2 X_3 X_4 + \bar{X}_1 X_2 \bar{X}_3 \bar{X}_4 + \bar{X}_1 X_2 \bar{X}_3 X_4 + \bar{X}_1 X_2 X_3 X_4 + X_1 \bar{X}_2 X_3 \bar{X}_4 + X_1 X_2 X_3 \bar{X}_4 + X_1 X_2 X_3 X_4$$

$$C = \bar{X}_1 \bar{X}_2 \bar{X}_3 X_4 + \bar{X}_1 X_2 \bar{X}_3 X_4 + \bar{X}_1 X_2 X_3 X_4 + X_1 \bar{X}_2 X_3 X_4 + X_1 X_2 X_3 X_4$$

Using K-maps to simplify the boolean expressions.

A

$X_1 \backslash X_2$	00	01	10	11
00	0	0	0	1
01	0	0	0	1
10	1	1	1	1
11	0	0	0	0

$$A = X_1 \bar{X}_2 \bar{X}_3 + X_2 X_4$$

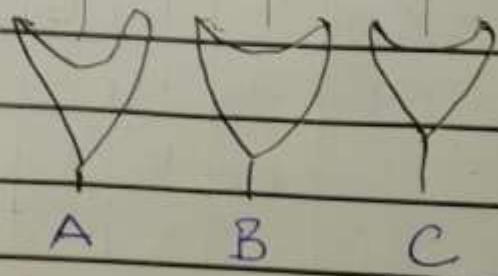
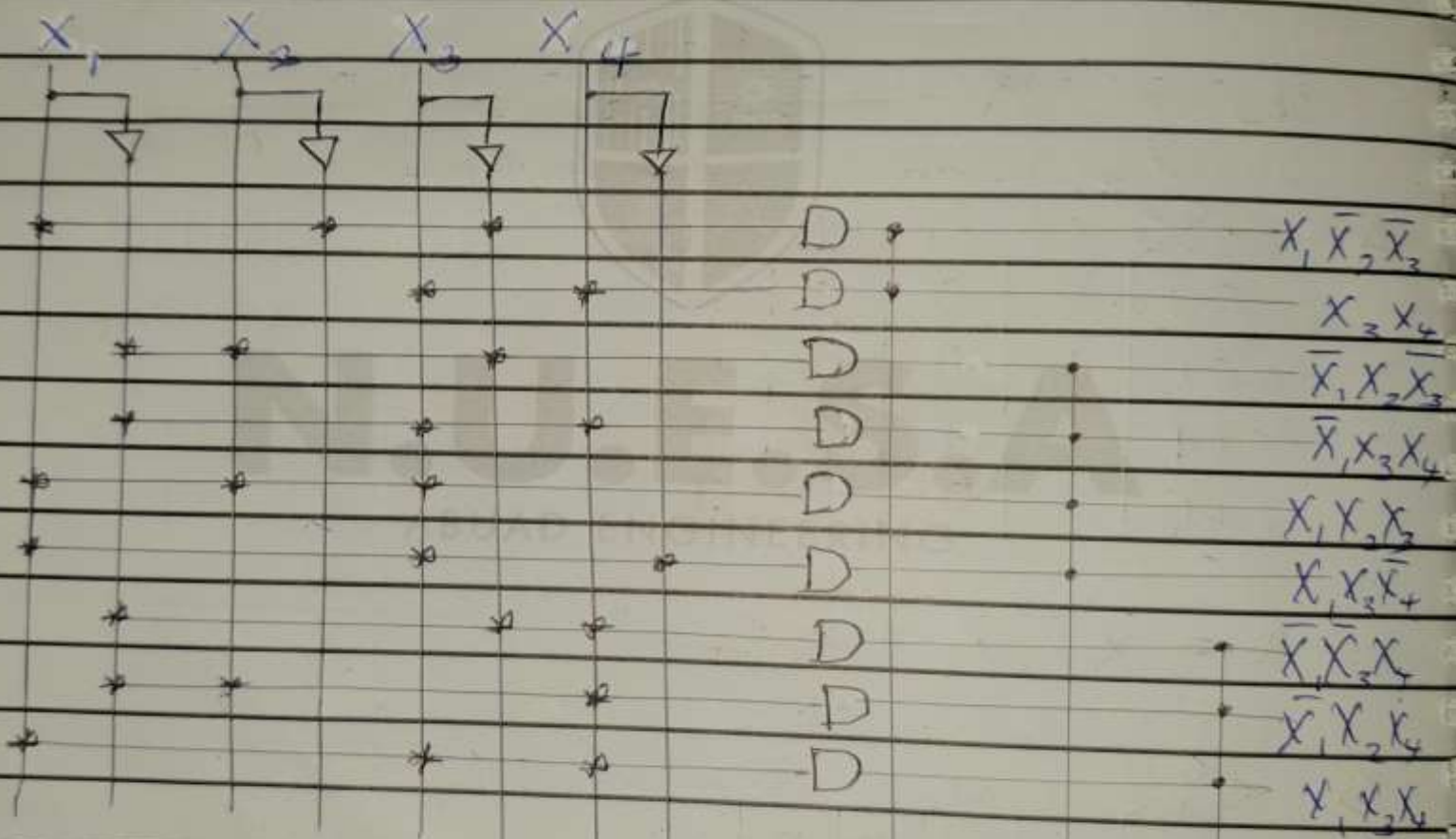
B

$X_1 \backslash X_2$	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	1	1	1	0
10	0	0	1	1

$$B = \bar{X}_1 X_2 \bar{X}_3 + \bar{X}_1 X_3 X_4 + X_1 X_2 X_3 + X_1 X_3 \bar{X}_4$$

C	$X_1 \backslash X_2$	00	01	11	10
	00	0	0	0	0
	01	1	1	0	0
	11	0	1	1	1
	10	0	0	0	0

$$C = \bar{X}_1 \bar{X}_3 X_4 + \bar{X}_1 X_2 X_4 + X_1 X_3 X_4$$



4 x 8 x 4 PLA

QUESTION 3

0 - closed

1 - Opened

Sw1	Sw2	Sw3	Sw4	OUTPUT (X)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	X
1	0	1	0	1
1	0	1	1	X
1	1	0	0	1
1	1	0	1	X
1	1	1	0	1
1	1	1	1	X

Simplifying the boolean

Using K-map

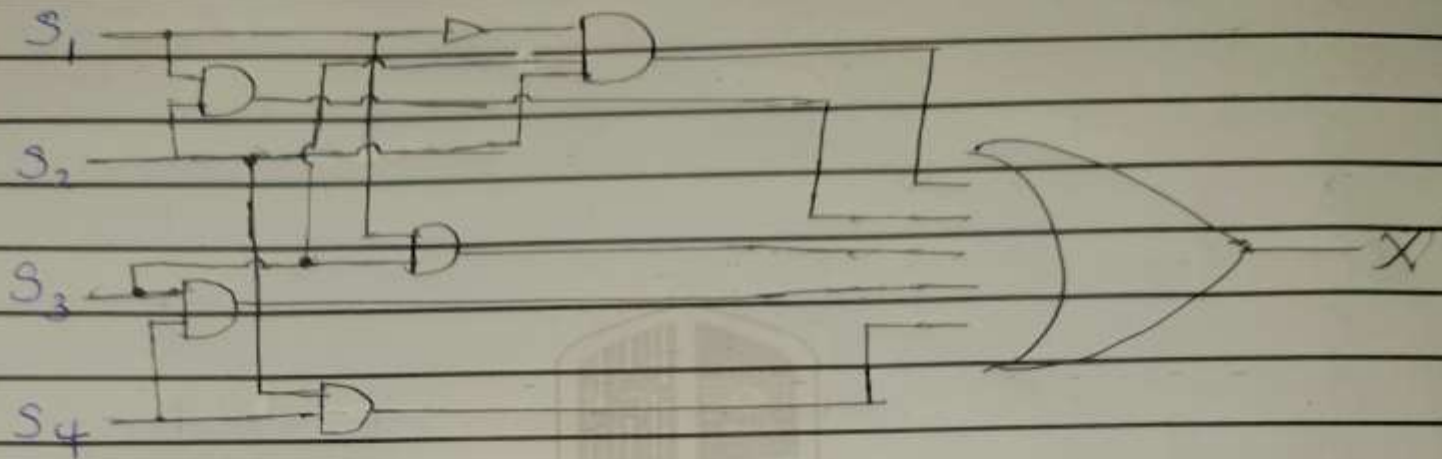
	$S_1 S_2$	00	01	11	10
$S_3 S_4$	00	0	0	1	0
	01	0	1	X	X
	11	1	1	X	X
	10	0	1	1	1

$$SW = S$$

$$X = S_1 S_2 + S_2 S_4 + S_3 S_4 + S_1 S_3 + \bar{S}_1 S_2 S_3$$

$$X = S_1 S_2 + S_2 S_4 + S_3 S_4 + S_1 S_3 + \overline{S_1} S_2 S_3$$

Circuit Diagram



VHDL Code

```

LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY Copymachine IS
    PORT (S1 : In std_logic;
          S2 : In std_logic;
          S3 : In std_logic;
          S4 : In std_logic;
          X : Out std_logic);
end Copymachine;
ARCHITECTURE synthesis1 OF Copymachine IS
    BEGIN
        X <= (S1 AND S2) OR (S2 AND S4) OR
              (S3 AND S4) OR (S1 AND S3)
              OR ((NOT S1) AND S2 AND S3);
    END synthesis1;

```