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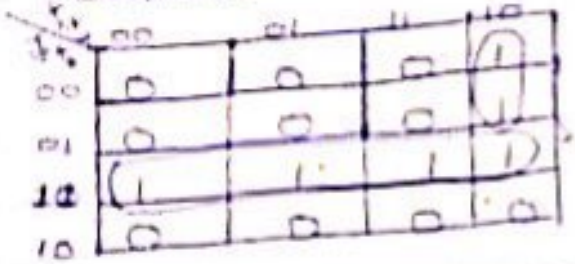
15/ENG02/016
Computer engineering

1) $A(x_1x_2x_3x_4) = \Sigma m(3,7,8,9,11,15)$
$B(x_1x_2x_3x_4) = \Sigma m(2,4,5,7,10,14,15)$
$C(x_1x_2x_3x_4) = \Sigma m(1,5,7,11,15)$

Truth Table:

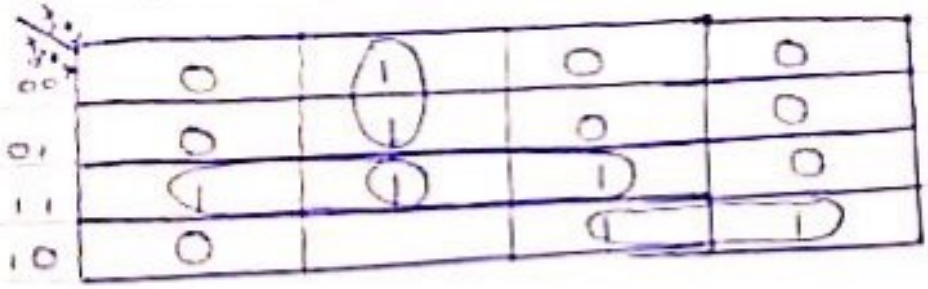
x_1	x_2	x_3	x_4	A	B	C
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	0
0	0	1	1	1	1	0
0	1	0	0	0	1	0
0	1	0	1	0	1	1
0	1	1	0	0	0	0
0	1	1	1	1	1	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	1	1	0
1	0	1	1	0	0	0
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	0	1	0
1	1	1	1	1	1	1

Output A:



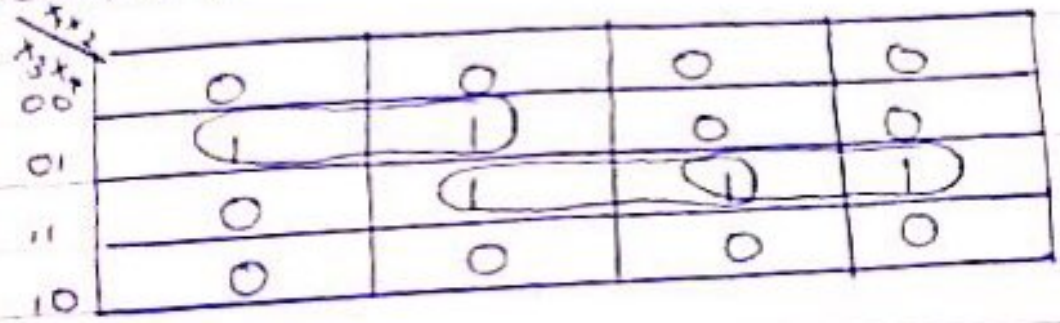
$A = x_1\bar{x}_2\bar{x}_3 + x_3x_4$

Output B:



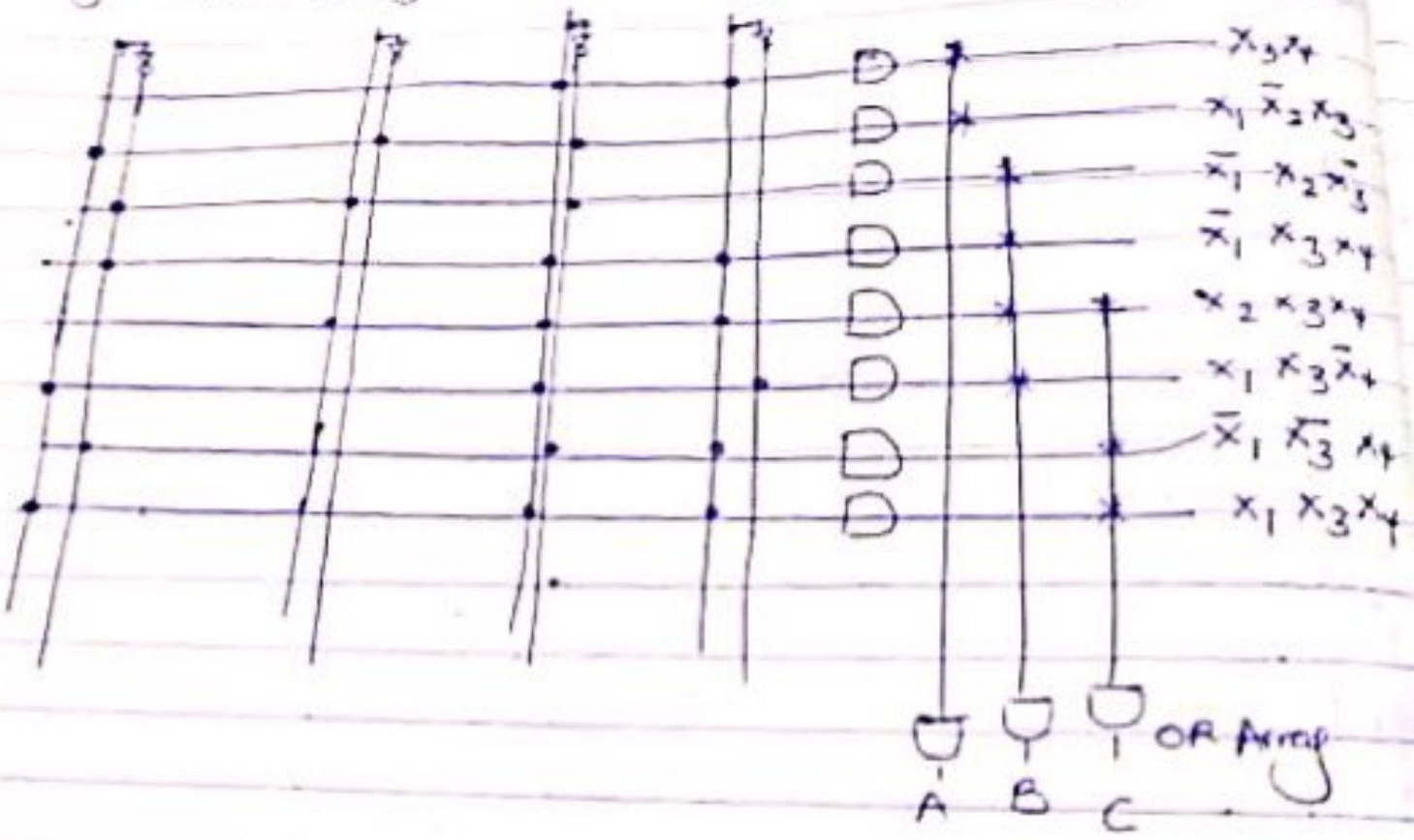
$B = \bar{x}_1x_2\bar{x}_3 + \bar{x}_1x_3x_4 + x_2x_3x_4 + x_1x_3\bar{x}_4$

Output C:



$C = \bar{x}_1\bar{x}_3x_4 + x_2x_3x_4 + x_1x_3x_4$

-> Logic Circuit Design: Implementing using PLA



Code:
Library ieee.
Use ieee.std_logic_1164.all;
Entity switches
Port (Swa, Swb, Swc, Swd : in
Std_logic; x : Out std_
logic);

End switches
Architecture data flow of switches is
begin
x <= (Swc and Swd) or
(SWa and Swb) or
(Swb and Swd) or
(Swa and Swc);
end data flow;

	00	01	11	10
00	0	0	1	0
01	0	1	x	x
11	1	1	x	x
10	0	1	1	1

$X = Sw_3 Sw_4 + Sw_1 Sw_2 + Sw_2 Sw_4 + Sw_1 Sw$