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Q1

A **[torus](https://en.m.wikipedia.org/wiki/Torus" \o "Torus) interconnect** is a switch-less [network topology](https://en.m.wikipedia.org/wiki/Network_topology" \o "Network topology) for connecting processing nodes in a [parallel computer](https://en.m.wikipedia.org/wiki/Parallel_computer" \o "Parallel computer) system.

A number of [supercomputers](https://en.m.wikipedia.org/wiki/Supercomputer" \o "Supercomputer) on the [TOP500](https://en.m.wikipedia.org/wiki/TOP500" \o "TOP500) list use three-dimensional torus networks, e.g. IBM's [Blue Gene/L](https://en.m.wikipedia.org/wiki/Blue_Gene" \l "Blue_Gene.2FL" \o "Blue Gene) and [Blue Gene/P](https://en.m.wikipedia.org/wiki/Blue_Gene" \l "Blue_Gene.2FP" \o "Blue Gene), and the [Cray](https://en.m.wikipedia.org/wiki/Cray" \o "Cray) XT3.[[1]](https://en.m.wikipedia.org/wiki/Torus_interconnect" \l "cite_note-Torus-1) IBM's [Blue Gene/Q](https://en.m.wikipedia.org/wiki/Blue_Gene" \l "Blue_Gene.2FQ" \o "Blue Gene) uses a five-dimensional torus network. Fujitsu's [K computer](https://en.m.wikipedia.org/wiki/K_computer" \o "K computer) and the [PRIMEHPC FX10](https://en.m.wikipedia.org/wiki/PRIMEHPC_FX10" \o "PRIMEHPC FX10) use a proprietary three-dimensional torus 3D mesh interconnect called Tofu.

**ADVANTAGES**

* Higher speed, lower latency

Because of the connection of opposite edges, data have more options to travel from one node to another which greatly increased speed.

* Better fairness

In a 4×4 mesh interconnect, the longest distance between nodes is from upper left corner to lower right corner. Each datum takes 6 hops to travel the longest path. But in a 4×4 Torus interconnect, upper left corner can travel to lower right corner with only 2 hops

* Lower energy consumption

Since data tend to travel fewer hops, the energy consumption tends to be lower.

### **DISADVANTAGES**

* Complexity of wiring

Extra wires can make the routing process in the physical design phase more difficult. If we want to lay out more wires on chip, it is likely that we need to increase the number of metal layers or decrease density on chip, which is more expensive. Otherwise, the wires that connect opposite edges can be much longer than other wires. This inequality of link lengths can cause problems because of [RC delay](https://en.m.wikipedia.org/wiki/RC_time_constant" \o "RC time constant).

* Cost

While long wrap-around links may be the easiest way to visualize the connection topology, in practice, restrictions on cable lengths often make long wrap-around links impractical. Instead, directly connected nodes—including nodes that the above visualization places on opposite edges of a grid, connected by a long wrap-around link—are physically placed nearly adjacent to each other in a folded torus network.[[5]](https://en.m.wikipedia.org/wiki/Torus_interconnect" \l "cite_note-5)[[6]](https://en.m.wikipedia.org/wiki/Torus_interconnect" \l "cite_note-6) Every link in the folded torus network is very short—almost as short as the nearest-neighbor links in a simple grid interconnect—and therefore low-latency.[[7]](https://en.m.wikipedia.org/wiki/Torus_interconnect" \l "cite_note-7)

**Q2**

[Hypercube](https://en.m.wikipedia.org/wiki/Hypercube" \o "Hypercube) networks are a type of [network topology](https://en.m.wikipedia.org/wiki/Network_topology" \o "Network topology) used to connect multiple [processors](https://en.m.wikipedia.org/wiki/Processors" \o "Processors) with memory modules and accurately route data. Hypercube networks consist of 2m nodes. These nodes form the vertices of squares to create an internetwork connection. A hypercube is basically a multidimensional [mesh network](https://en.m.wikipedia.org/wiki/Mesh_networking" \o "Mesh networking) with two nodes in each dimension. Due to similarity, such topologies are usually grouped into a k-ary d-dimensional mesh topology family where d represents the number of dimensions and k represents the number of nodes in each dimension.