Phase-Locked Loop (PLL) Fundamentals

By **Ian Collins**

Abstract:

Phase-locked loop (PLL) circuits exist in a wide variety of high frequency applications, from simple clock clean-up circuits, to local oscillators (LOs) for high performance radio communication links, and ultrafast switching frequency synthesizers in vector network analyzers (VNA). This article explains some of the building blocks of PLL circuits with references to each of these applications, in turn, to help guide the novice and PLL expert alike in navigating part selection and the trade-offs inherent for each different application. The article references the Analog Devices ADF4xxx and HMCxxx family of PLLs and voltage controlled oscillators (VCOs), and uses ADIsimPLL (Analog Devices in-house PLL circuit simulator) to demonstrate these different circuit performance parameters.

Basic Configuration: Clock Clean-Up Circuit

In its most basic configuration, a phase-locked loop compares the phase of a reference signal (F_{REF}) to the phase of an adjustable feedback signal (RF_{IN}) F_0, as seen in Figure 1. In Figure 2 there is a negative feedback control loop operating in the frequency domain. When the comparison is in steady-state, and the output frequency and phase are matched to the incoming frequency and phase of the error detector, we say that the PLL is locked. For the purposes of this article we shall only consider a classical digital PLL architecture as implemented on the Analog Devices ADF4xxx family of PLLs.

The first essential element in this circuit is the phase frequency detector (PFD). The PFD compares the frequency and phase of the input to REF_{IN} to the frequency and phase of the feedback to RF_{IN}. The ADF4002 is a PLL that can be configured as a standalone PFD (with the feedback divider N = 1). As such, it can be used with a high quality voltage controlled crystal oscillator (VCXO) and a narrow low-pass filter to clean up a noisy REF_{IN} clock.

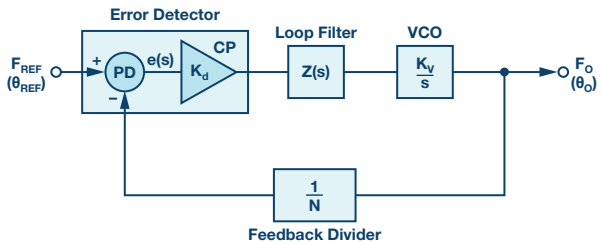

Figure. 1 Basic PLL configuration.

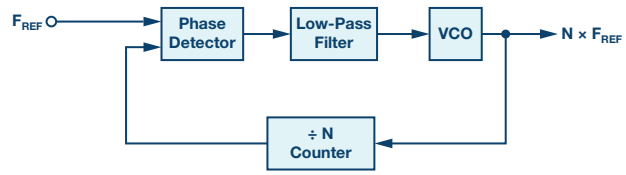

Figure 2. Basic PLL configuration.

Phase Frequency Detector

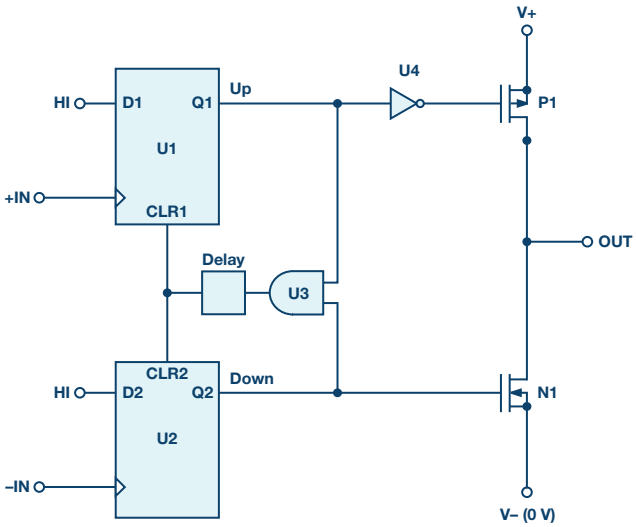

Figure 3. Phase frequency detector.

The phase frequency detector in Figure 3 compares the input to F_{REF} at +IN and the feedback signal at –IN. It uses two D-type flip flops with a delay element. One Q output enables a positive current source, and the other Q output enables a negative current source. These current sources are known as the charge pump. For more details on PFD operation, consult "Phase-Locked Loops for High Frequency Receivers and Transmitters."

Using this architecture, the input to +IN below is at a higher frequency than the –IN (Figure 4), and the resultant charge pump output is pumping current high, which, when integrated in the PLL low-pass filter, will push the tuning voltage of the VCO up. In this way, the –IN frequency will increase as the VCO increases, and the two PFD inputs will eventually converge or lock to the same frequency (Figure 5). If the frequency to –IN is higher than +IN, the reverse happens.

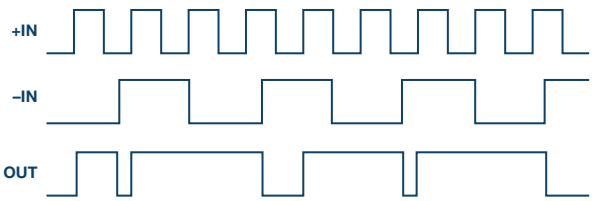

Figure 4. A PFD out of phase and frequency lock.

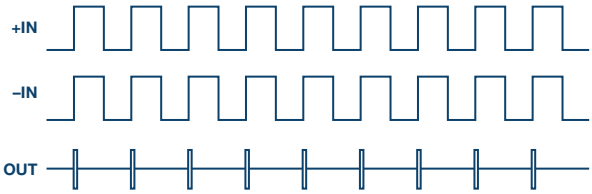

Figure 5. Phase frequency detector, frequency, and phase lock.

Returning to our original example of the noisy clock that requires cleaning, the phase noise profile of the clock, free running VCXO, and closed-loop PLL can be modeled in ADIsimPLL.

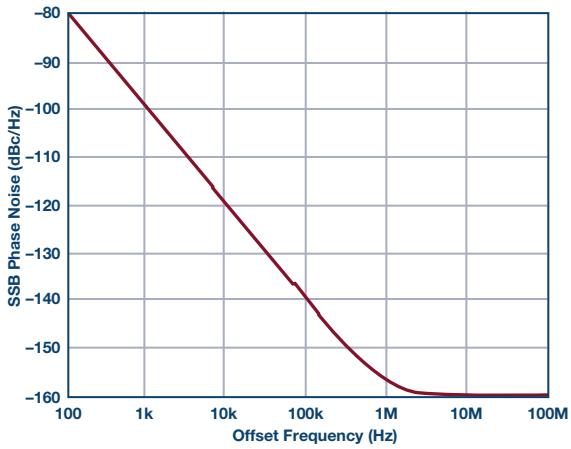

Figure 6. Reference noise.

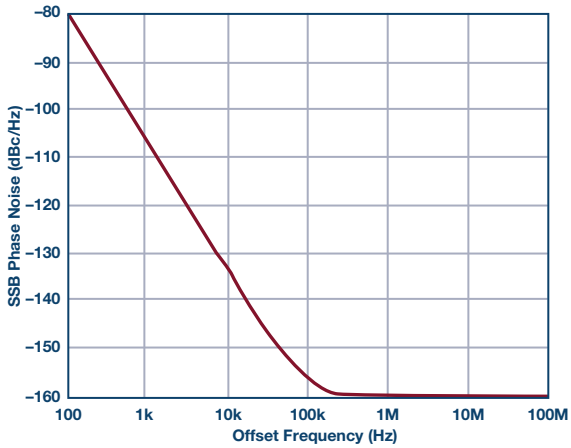

Figure 7. Free running VCXO.

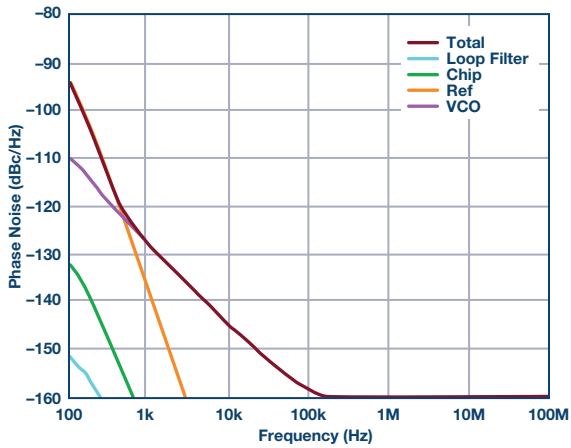

Figure 8. Total PLL noise.

As can be seen with the ADIsimPLL plots shown, the noisy phase noise profile of the REF_{IN} (Figure 6) is filtered by the low-pass filter. All the in-band noise contributed by the PLL reference and PFD circuitry is filtered out by the low-pass filter, leaving only the much lower VCXO noise (Figure 7) outside the loop bandwidth (Figure 8). When the output frequency is equal to the input frequency it creates one of the simplest PLL configurations. Such a PLL is called a clock clean-up PLL. For clock clean-up applications such as these, narrow (<1 kHz) low-pass filter bandwidths are recommended.

High Frequency Integer-N Architecture

To generate a range of higher frequencies, a VCO is used, which tunes over a wider range than a VCXO. This is regularly used in frequency hopping or in spread spectrum frequency hopping (FHSS) applications. In such PLLs, the output is a high multiple of the reference frequency. Voltage controlled oscillators contain a variable tuning element, such as a varactor diode, which varies its capacitance with input voltage, allowing a tuneable resonant circuit, which permits a range of frequencies to be generated (Figure 9). The PLL can be thought of as a control system for this VCO.

A feedback divider is used to divide the VCO frequency to the PFD frequency, which allows a PLL to generate output frequencies that are multiples of the PFD frequency. A divider may also be used in the reference path, which permits higher frequency references to be used than the PFD frequency. A PLL like this is the ADF4108 from Analog Devices. The PLL counters are the second essential element to be considered in our circuit.

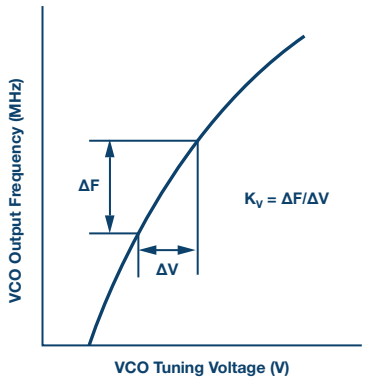

Figure 9. Voltage controlled oscillator.

The key performance parameters of PLLs are phase noise, unwanted by-products of the frequency synthesis process, or spurious frequencies (spurs for short). For integer-N PLLs, spurious frequencies are generated by the PFD frequency. A leakage current from the charge pump will modulate the tuning port of the VCO. This effect is lessened by the low-pass filter and the narrower this is, the greater the filtering of the spurious frequency. An ideal tone would have no noise or additional spurious frequency (Figure 10), but in practice phase noise appears as a skirtaround a carrier, as shown in Figure 11. Single sideband phase noise is the relative noise power to the carrier in a 1 Hz bandwidth, specified at a frequency offset from the carrier.

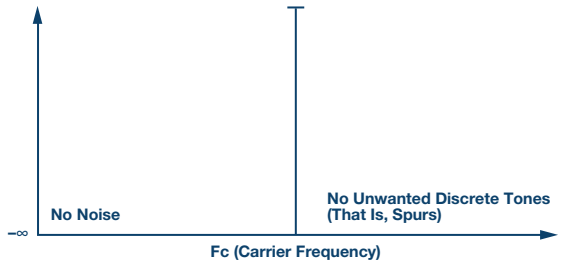

Figure 10. Ideal LO spectrum.

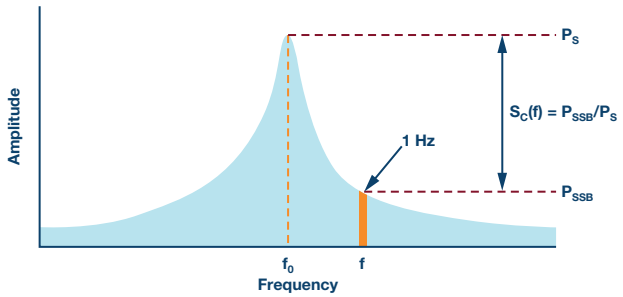

Figure 11. Single sideband phase noise.

Integer-N and Fractional-N Divider

For narrow-band applications, the channel spacing is narrow (typically <5 MHz) and the feedback counter, N, is high. Gaining high N values with a small circuit is achieved by the use of a dual modulus P/P + 1 prescaler, as seen in Figure 12, and allows N values to be computed with the calculation of N = PB + A, which, using the example of an 8/9 prescaler and an N value of 90, computes a value of 11 for B and 2 for A. The dual modulus prescaler will divide by 9 for A or two cycles. It will then divide by 8 for the remaining (B-A) or 9 cycles, as described in Table 1. The prescaler is generally designed using a higher frequency circuit technology, such as bipolar emitter coupled logic (ECL) circuits, while the A and B counters can take this lower frequency prescaler output and can be manufactured with lower speed CMOS circuitry. This reduces circuit area and power consumption. Low frequency clean up PLLs like the ADF4002 omit this prescaler.

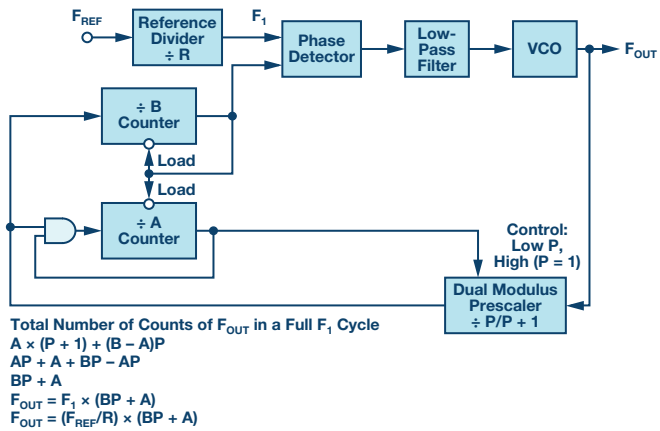

Figure 12. PLL with dual modulus N counter.

Table 1. Dual Modulus Prescaler Operation

N Value	P/P + 1	B Value	A Value
90	9	11	2
81	9	10	1
72	8	9	0
64	8	8	0
56	8	7	0
48	8	6	0
40	8	5	0
32	8	4	0
24	8	3	0
16	8	2	0
8	8	1	0
0	8	0	0

The in-band (inside the PLL loop filter bandwidth) phase noise is directly influenced by the value of N, and in-band noise is increased by 20log (N). So, for narrow-band applications in which the N value is high, the in-band noise is dominated by the high N value. A system that permits a much lower N value, but still permits fine resolution is enabled by a fractional-N synthesizer, such as the ADF4159 or HMC704. In this manner, the in-band phase noise can be greatly reduced. Figures 13 through 16 illustrate how this is achieved. In these examples, two PLLs are used to generate frequencies suitable for a 5G systems local oscillator (LO) in a range between 7.4 GHz to 7.6 GHz, with 1 MHz of channel resolution. The ADF4108 is used in an integer-N configuration (Figure 13) and the HMC704 is used in a fractional-N configuration. The HMC704 (Figure 14) can be used with a 50 MHz PFD frequency, which lowers the N value and, hence, the in-band noise, while still permitting a 1 MHz (or indeed smaller) frequency step size—an improvement of 15 dB (at 8 kHz offset frequency) is noted (Figure 15 vs. Figure 16). The ADF4108, however, is forced to use a 1 MHz PFD to achieve the same resolution.

Care needs to be taken with fractional-N PLLs to ensure that spurious tones do not degrade system performance. On PLLs such as the HMC704, integer boundary spurs (generated when the fractional portion of the N value approaches 0 or 1, like 147.98 or 148.02 are very close to the integer value of 148) generate the most concern. This can be mitigated by buffering the VCO output to the RF input, and/or careful frequency planning in which the REF_{IN} can be changed to avoid these more problematic frequencies.

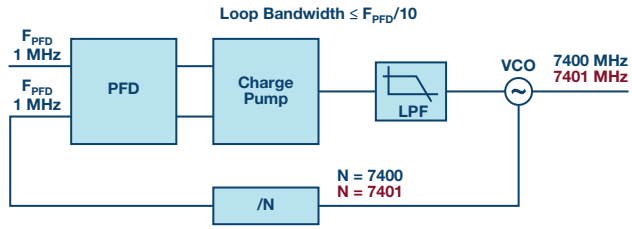

Figure 13. Integer N PLL.

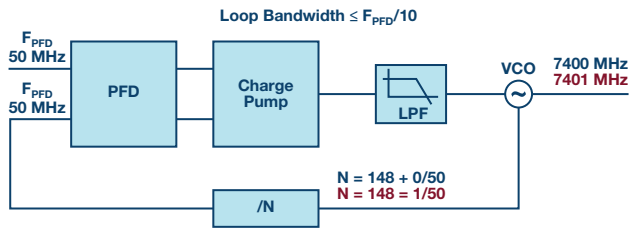

Figure 14. Fractional-N PLL.

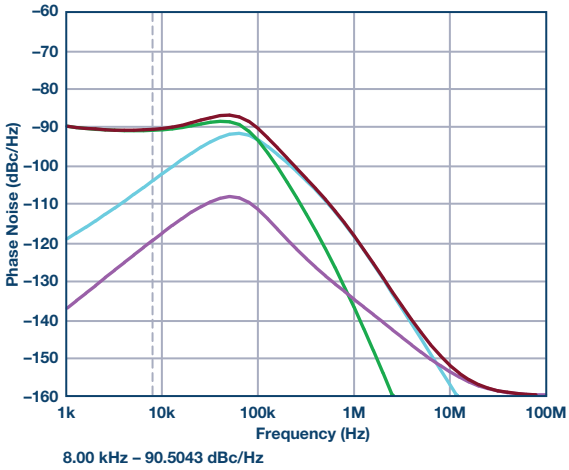

Figure 15. Integer N PLL in-band phase noise.

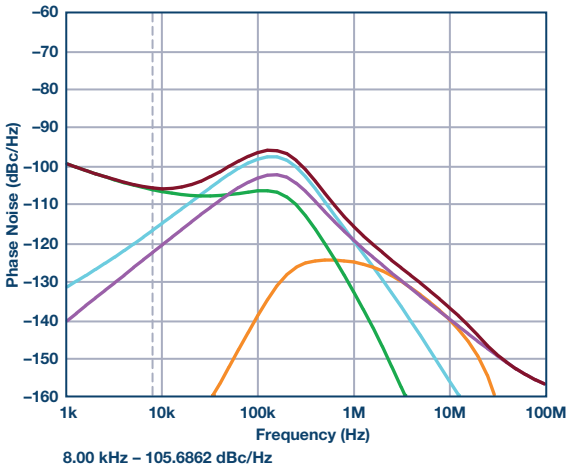

Figure 16. Fractional-N PLL in-band phase noise.

For the majority of PLLs the in-band noise is highly dependent on the N value, and also on the PFD frequency. Subtracting 20log (N) and 10log (F_{PFD}) from the flat portion of an in-band phase noise measurement yields the figure of merit (FOM). A common metric for choosing PLLs is to compare the FOM. Another factor that influences the in-band noise is the 1/f noise, which is dependent on the output frequency of the device. The FOM contribution and the 1/f noise, together with the reference noise, dominate the in-band noise of a PLL system.

Narrow-Band LO for 5G Communications

For communication systems, the chief specifications from the PLL perspective are error vector magnitude (EVM) and VCO blocking specifications. EVM is similar in scope to integrated phase noise, which considers the noise contribution over a range of offsets. For the 5G system listed earlier, the integration limits are quite wide, starting at 1 kHz and continuing to 100 MHz. EVM can be thought of as a percentage degradation of a perfectly modulated signal from its ideal point expressed as a percentage (Figure 17). In a similar manner, integrated phase noise integrates the noise power at different offsets from the carrier and expresses this can be configured to calculate the EVM, integrated phase noise, and rms phase error and jitter. Modern signal source analyzers will also include these numbers at the push of a button (Figure 18). As modulation schemes increase in density, EVM becomes critical. For 16-QAM, the required minimum EVM according to ETSI specification 3GPP TS 36.104 is 12.5%. For 64-QAM, the requirement is 8%. However, since EVM is comprised of various other nonideal parameters due to power amplifier distortion and unwanted mixer products, the integrated noise (in dBc) is usually defined separately.

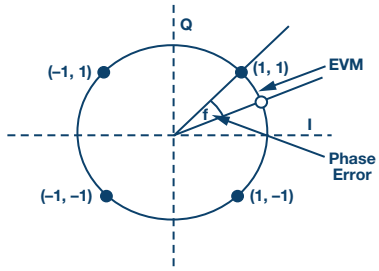

Figure 17. Phase error visualization.

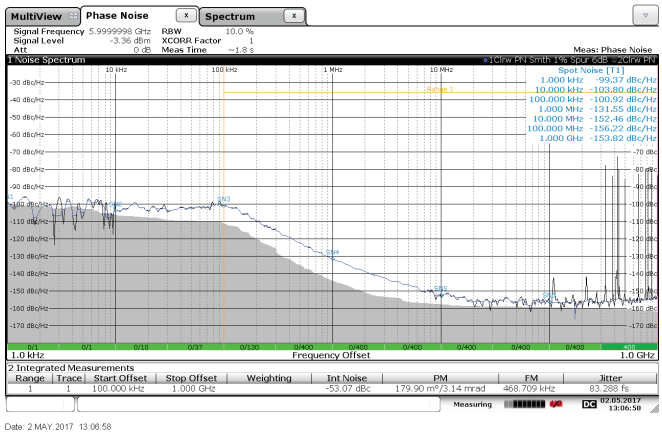

Figure 18. Signal source analyzer plot.

VCO blocking specifications are very important in cellular systems that need to account for the presence of strong transmissions. If a receiver signal is weak, and if the VCO is too noisy, then the nearby transmitter signal can mix down and drown out the wanted signal (Figure 19). The illustration in Figure 19 demonstrates how the nearby transmitter (800 kHz away) transmitting at –25 dBm power could, if the receiver VCO is noisy, swamp the wanted signal at –101 dBm. These specifications form part of a wireless communications standard. The blocking specifications directly influence the performance requirement of the VCO.

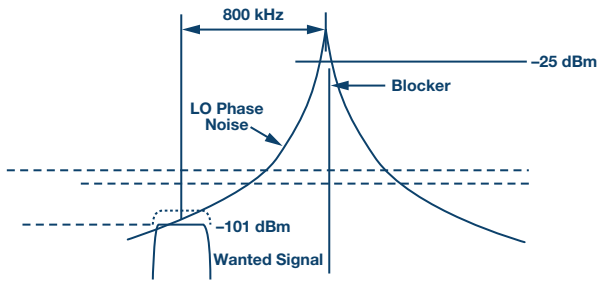

Figure 19. VCO noise blockers.

Voltage Controlled Oscillators (VCOs)

The next PLL circuit element to be considered in our circuit is the voltage controlled oscillator. With VCOs, a fundamental trade-off between phase noise, frequency coverage, and power consumption is necessary. The higher the quality factor (Q) of the oscillator, the lower the VCO phase noise is. However, higher Q circuits have narrower frequency ranges. Increasing the power supply will also lower the phase noise. Looking at the Analog Devices family of VCOs, the HMC507 covers a range of 6650 MHz to 7650 MHz and the VCO noise at 100 kHz is approximately –115 dBc/Hz. By contrast, the HMC586 covers a full octave from 4000 MHz to 8000 MHz, but has higher phase noise of –100 dBc/Hz. One strategy for minimizing phase noise in such VCOs is to increase the voltage tuning range of the V_{TUNE} to the VCO (up to 20 V or greater). This increases PLL circuit

complexity, as most PLL charge pumps can only tune to 5 V, so an active filter using operational amplifiers is used to increase the tuning voltage of the PLL circuit on its own.

Multiband Integrated PLLs and VCOs

Another strategy to increase frequency coverage without degrading VCO phase noise is to use a multiband VCO, in which overlapping frequency ranges are used to cover an octave of frequency range, and lower frequencies can be generated by using frequency dividers at the output of the VCO. Such a device is the ADF4356, which uses four main VCO cores each with 256 overlapping frequency ranges. The internal reference and feedback frequency dividers are used by the device to choose the appropriate VCO band, a process known as VCO band select or autocalibration.

The wide tuning range of the multiband VCOs makes them suitable for use in wideband instrumentation, in which they generate a wide range of frequencies. The 39 bits of fractional-N resolution also makes them ideal candidates for these precise frequency applications. In instruments such as vector network analyzers, ultrafast switching speed is essential. This can be achieved by using a very wide low-pass filter bandwidth, which tunes to final frequency very quickly. The automatic frequency calibration routine can be bypassed in these applications by using a look-up table with the frequency values directly programmed for each frequency, true single core wideband VCOs like the HMC733 can also be used with less complexity.

For phase-locked loop circuits, the bandwidth of the low-pass filter has a direct influence on the settling time of the system. The low-pass filter is the final element in our circuit. If settling time is critical, the loop bandwidth should be increased to the maximum bandwidth permissible for achieving stable lock and meeting phase noise and spurious frequency targets. The narrow-band demands in a communications link mean the optimal bandwidth of the low-pass filter for minimum integrated noise (between 30 kHz to 100 MHz) is about 207 kHz (Figure 20) using the HMC507. This provides approximately –51 dBc of integrated noise and achieves frequency lock to within 1 kHz error in about 51 µs (Figure 22).

By contrast, the wideband HMC586 (covering from 4 GHz to 8 GHz) achieves the optimum rms phase noise with a wider bandwidth closer to 300 kHz bandwidth (Figure 21), achieving –44 dBc of integrated noise. However, it achieves frequency lock to the same specification in less than 27 µs (Figure 23). Correct part selection and the surrounding circuit design are all critical for achieving the best outcome for the application.

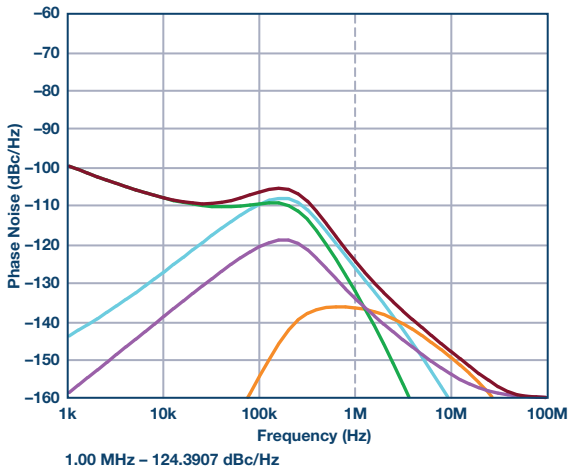

Figure 20. Phase noise HMC704 plus HMC507.

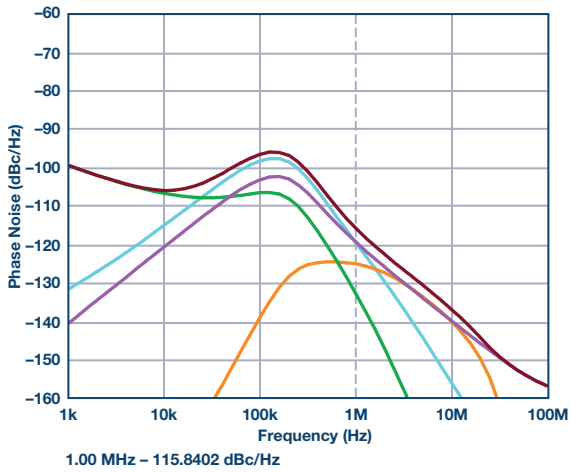

Figure 21. Phase noise HMC704 plus HMC586.

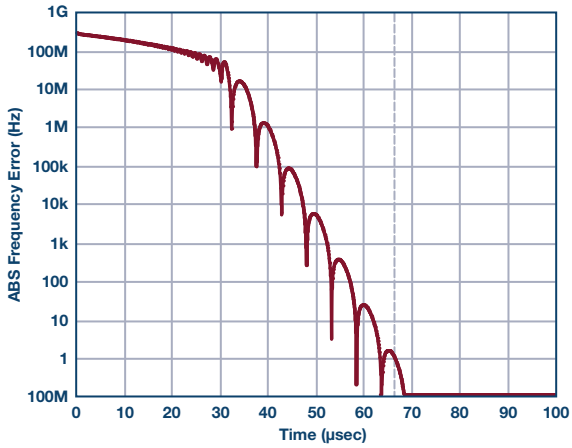

Figure 22. Frequency settling: HMC704 plus HMC507.

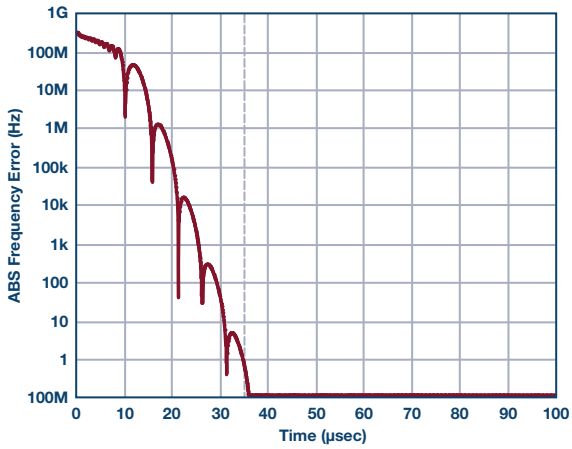

Figure 23. HMC704 plus HMC586.

Low Jitter Clocking

For high speed digital-to-analog converters (DACs) and high speed analog-to-digital converters (ADCs), a clean low jitter sampling clock is an essential building block. To minimize in band noise a low N value is desired; but to minimize spurious noise, integer N is preferred. Clocking tends to be fixed frequency so the frequencies can be chosen to ensure

that the REF_{IN} frequency is an exact integer multiple of the input frequency. This ensures the lowest in-band PLL noise. The VCO (whether integrated or not) needs to be chosen to ensure that it is sufficiently low noise for the application, paying particular attention to the wideband noise. The low-pass filter then needs to be carefully placed to ensure that the in-band PLL noise will intersect with the VCO noise—this ensures lowest rms jitter. A low-pass filter with phase margin of 60° ensures lowest filter peaking, which minimizes jitter. In this manner, low jitter clocking falls in between the clock clean-up application of the first circuit discussed in this article, and the fast switching capability of the last circuit discussed.

For clocking circuits, the rms jitter of the clock is the key performance parameter. This can be estimated using ADIsimPLL or measured with a signal source analyzer. For high performance PLL parts like the ADF5356, a relatively wide low-pass filter bandwidth of 132 kHz, together with an ultralow REF_{IN} source like a Wenxel OCXO, allows the user to design clocks with rms jitter below 90 fs (Figure 26). Manipulating the placement of the PLL loop filter bandwidth (LBW) shows how decreasing it too much has an effect in which VCO noise begins to dominate at small offsets (Figure 24) where the in-band PLL noise would in fact be lower, and increasing it too much means the in-band noise is dominating at offsets where the VCO noise would instead be significantly lower (Figure 25).

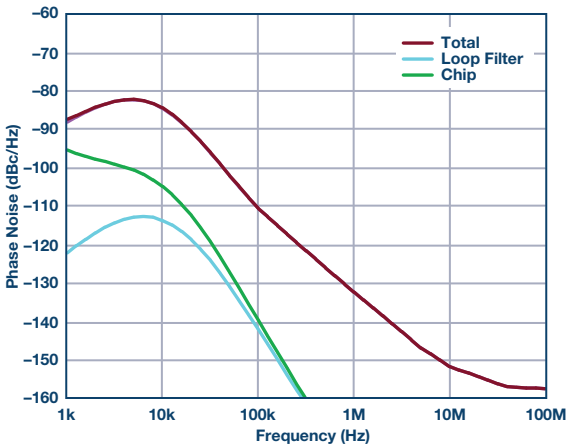

Figure 24. LBW = 10 kHz, 331 fs jitter.

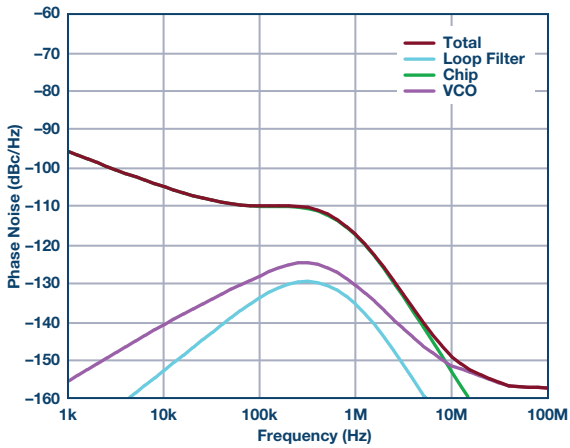

Figure 25. LBW = 500 kHz, 111 fs jitter.

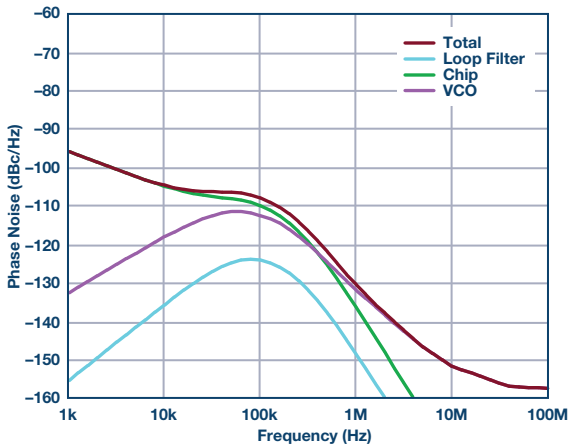

Figure 26. LBW = 132 kHz, 83 fs jitter.

References

Collins, Ian. "Integrated PLLs and VCOs for Wireless Applications." *Radio Electronics*, 2010.

Curtin, Mike and Paul O'Brien. "Phase-Locked Loops for High Frequency Receivers and Transmitters." *Analog Dialogue*, Vol. 33, 1999.

Ian Collins [ian.collins@analog.com] graduated from University College Cork with a degree in electrical and electronic engineering and has worked in the RF and Microwave Group of Analog Devices since 2000. He is currently applications manager of the Microwave Frequency Generation Group, which focuses mainly on phase-locked loop (PLL) and voltage controlled oscillator (VCO) products. When not spending time at work or with his young family, Ian enjoys photography and the theater (both on- and off-stage), reading, and listening to music.

Ian Collins