Q1b. p94 HALF ADDERS

The truth table for the half adder is shown below: The numbers being added are on the input side of the table. These are A and B input columns. The truth table needs two output columns, one column for the sum and one column for the carry.

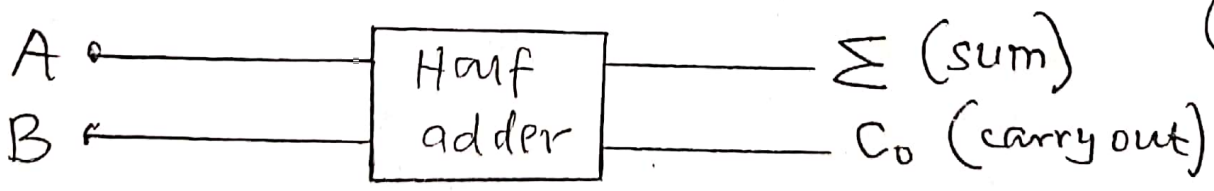
The sum column is labeled with the summation symbol Σ. The carry column is labeled with a C_0. The C_0 stands for carry output or carry out.

INPUTS		OUTPUTS	
B	A	Σ	C_0
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1
Binary digits to be added		sum	carry out
		XOR	AND

(a) Truth Table.

A convinient block symbol for the adder that performs the job of the truth table is shown below.

(b)



This circuit is called a half-adder circuit.

e half-adder circuit has two inputs (A·B) and two outputs, (Σ, C_o).

Take a careful look at the half-adder truth table, What is the Boolean expression needed for C_o output? The Boolean expression is

$$A \cdot B = C_o$$

You need a two-input AND gate to take care of output C_o.

Now what is the Boolean expression for the sum (Σ) output of the half-adder in the Truth table?

The Boolean expression is $\bar{A} \cdot B + A \cdot \bar{B} = \Sigma$. Two AND gates, two inverters, and one "OR" gate will do the job. If you look closely, you will notice that this pattern is also that of an "XOR" gate.

From the table.

	Σ
1st column: $\bar{A}B + A\bar{B}$ 1·0 + 01 0 + 0 = 0	0
2nd column: $\bar{A}B + A\bar{B}$ 00 + 11 0 + 1 = 1	1
3rd column: $\bar{A}B + A\bar{B}$ 11 + 00 1 + 0 = 1	1
4th column: $\bar{A}B + A\bar{B}$ 01 + 10 = 1	0

Simplified Boolean expression is then 3 (c)

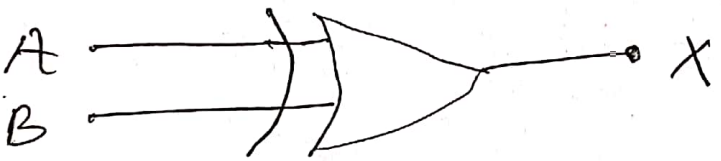
$A \oplus B = \Sigma$.

In other words, we find that only one 2-input XOR gate is needed to produce the sum output.

Recall: THE EXCLUSIVE-OR GATE.

The XOR gate has only two inputs. The exclusive-OR gate output is "High" only when the two inputs are at opposite logic levels. This operation can be stated as follows with reference to inputs A and B and output X.

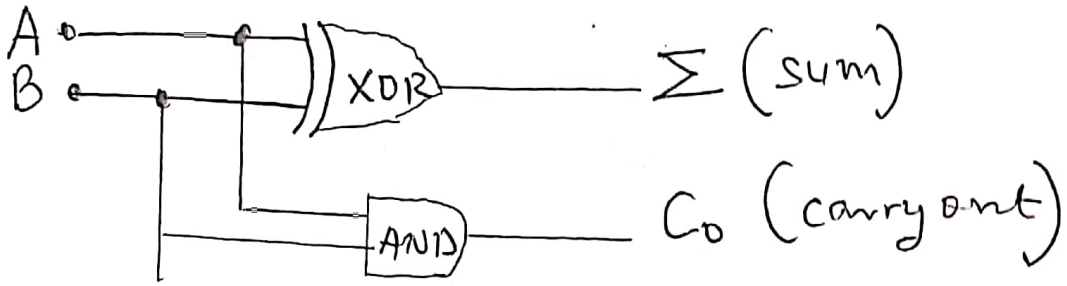
A	B	X – outputs
0	0	0
0	1	1
1	0	1
1	1	0



XOR.

ng a two-input AND gate and a two-input (Δ)
OR gate, a logic symbol diagram for a
alf adder is shown below.

HALF ADDER



FULL ADDERS

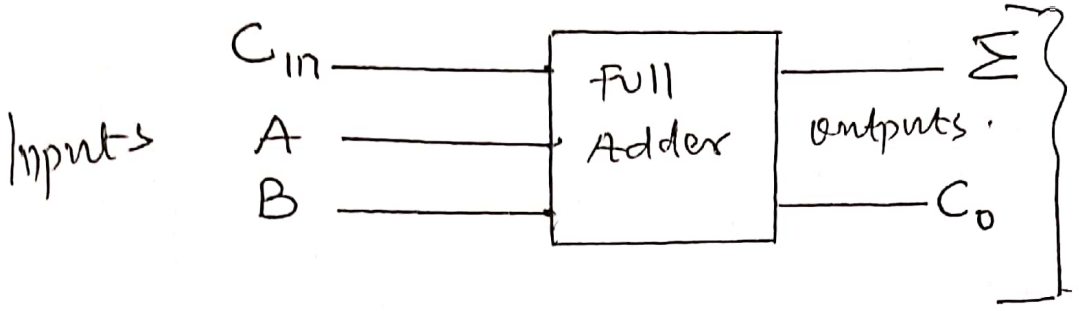
The truth table for a full adder is shown below.
ne full adder must be used when it is possible to have an
itral "carry input".

INPUTS			OUTPUTS	
C_{in}	B	A	Σ	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1
CARRY + B + A			SUM	CARRY OUT

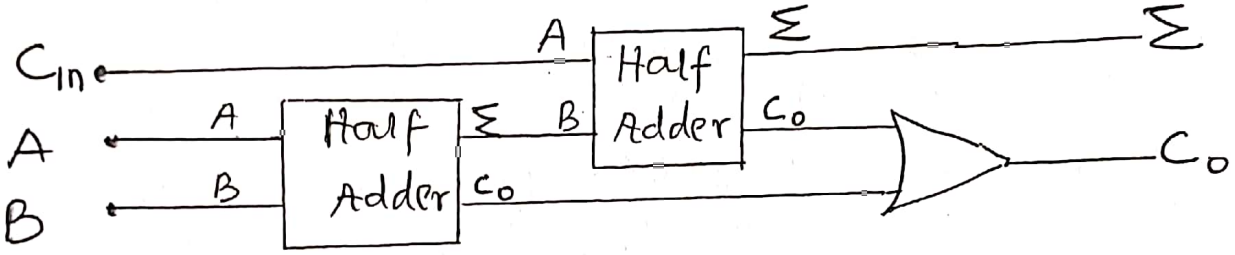
Truth Table
full Adder.

block diagram of a full adder is shown below. The full adder has three inputs: Σ (E)

C_{in}, A, and B. These three inputs must be added to get the Σ and C_o outputs.



(b) Block Diagram full Adder.



(c) constructed from half adders and an "OR" gate

ne of the easiest methods of forming the combinational ogic for a full adder is shown in fig c above. wo half-adder circuits and an OR gate are used. he expression for this arrangement is:

$$A \oplus B \oplus C = \Sigma$$

he expression for the carry out is:

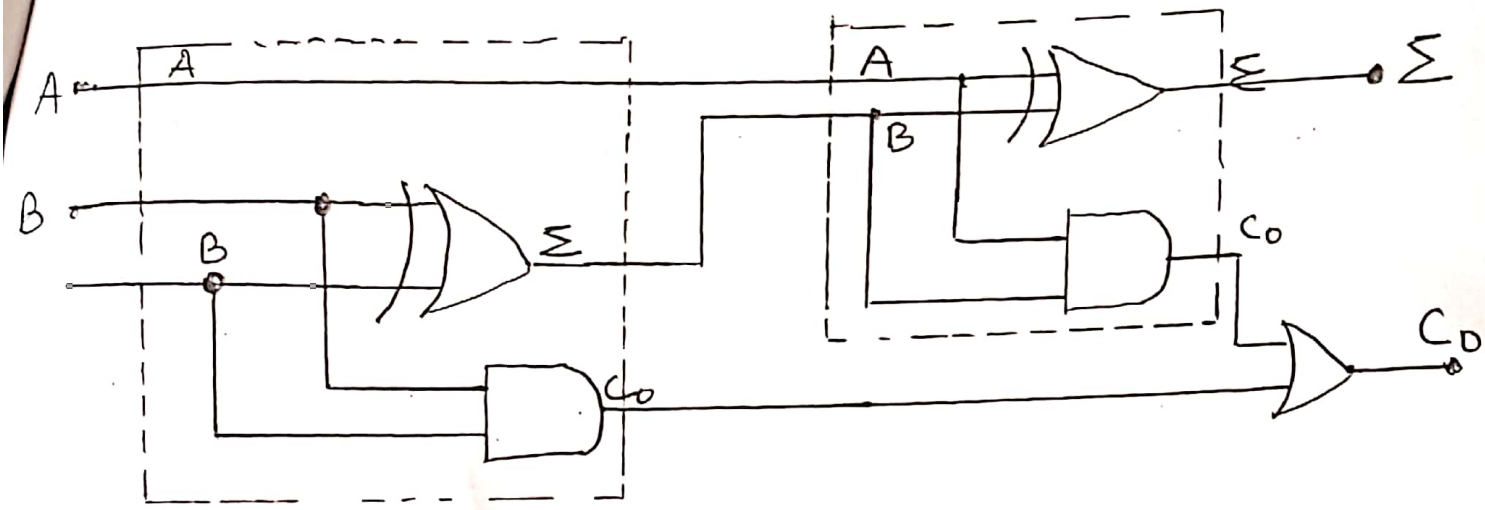
$$A \cdot B + C_{in} \cdot (A \oplus B) = C_o$$

Explain !!! In class.

diagram below is a full-adder logic circuit.

(F) 6

FULL ADDER LOGIC DIAGRAM



Many circuits similar to half and full adders are part of a microprocessor's arithmetic – logic unit (ALU). These circuits are then used for adding 8-bit or 16- or 32-bit binary number in a microcomputer system.

JM